The Field-effect transistor (FET)

We know that the ***bipolar junction transistor*** or ***BJT*** is a ***current controlled device***.

The ***FET*** or ***field effect transistor*** is a ***voltage controlled device.***

The output current of the FET is controlled by an input voltage, not an input current.

There are two basic types of FET's:

- The junction field effect transistor or JFET
- the metal oxide FET or MOSFET.

We will look at the variations and limitations of both types of devices.

Introduction to the JFET

The physical construction of the JFET is significantly different than the BJT.

The diagram to the right is the first step in making an n-channel JFET.

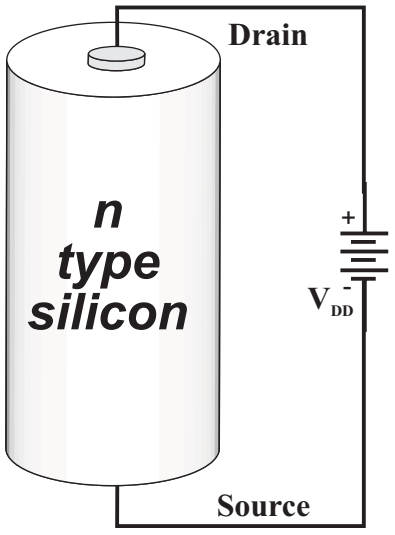


Figure 1 - The beginnings of an n-Channel JFET.

It is a single piece of n-type silicon semi-conductor, with a terminal fused to each end.

The lower end is called a ***source*** & the upper end is called a ***drain***

The supply voltage V_{DD} forces conventional current to flow from the drain to the source.

The JFET

To complete our JFET, we will add p-type material as shown in Figure 2. It will be in the shape of a collar and surrounds the original n-type silicon.

As you can see, there is a channel of n-type material that passes through the collar, hence the name n-channel JFET. The third terminal, called the *gate*, is attached to the collar.

Remember that the JFET is made from one solid piece of intrinsic silicon that has been doped to achieve the configuration shown in Figure 2.

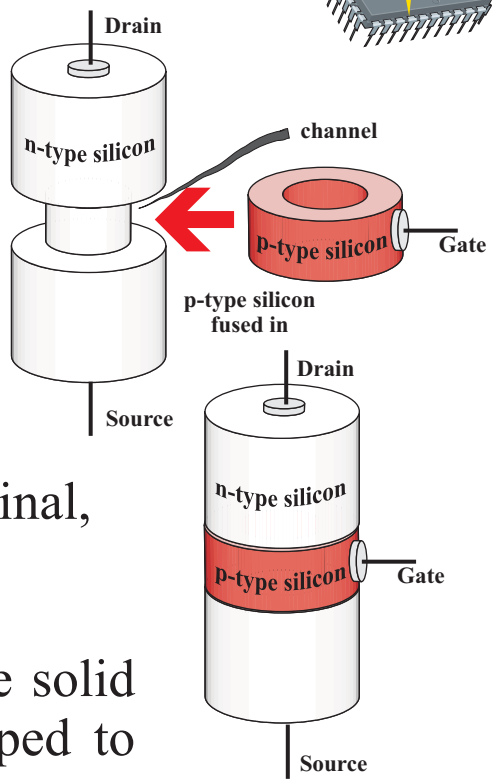


Figure 2 - The n Channel JFET

Where the n-type and p-type materials meet, a diode junction forms. A depletion layer forms in a similar fashion to the pn junction that we studied last term. This pn junction has an important function in the operation of the JFET.

The p-Channel JFET

The p-channel JFET is made in a similar fashion to the n-channel variety, however in this case, the channel is p-type material and the gate ring is n-type material as shown in Figure 3.

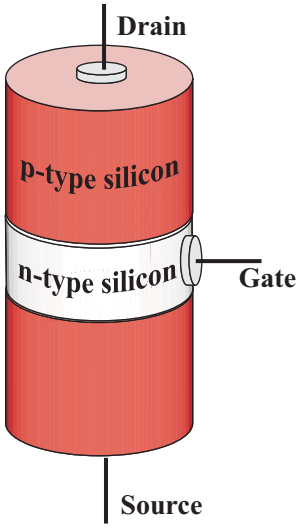
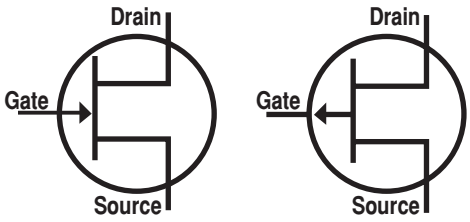


Figure 3 - The p Channel JFET

As with the pnp type transistor, all the voltages and currents switch polarity when working with this device.

The Schematic Symbols



The schematic symbols are shown to the left. Note that the gate arrow points out for the p-channel and in for the n-channel.

The circle is optional as with the BJT.

The operation of the JFET is relatively simple.

Figure 4 shows a cross section of the JFET. The voltage source V_{DS} generates the current through the channel. The voltage source V_{GS} is used to control this current.

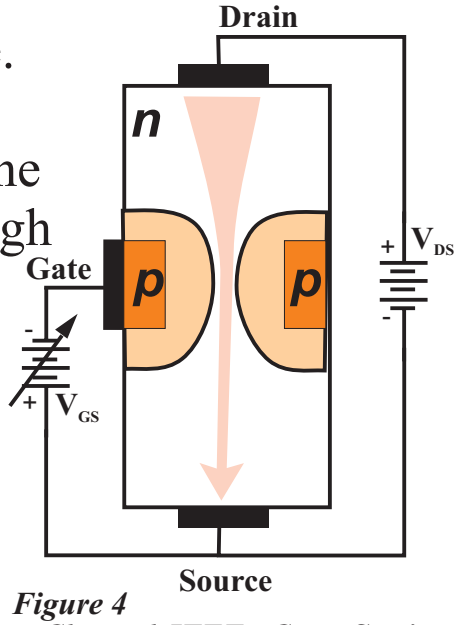


Figure 4
n-Channel JFET - Cross Section

How it Works - Controlling I_D

The overall operation of the JFET is based on the ***varying width of the channel*** to control the drain current.

In Figure 5, the voltage V_{DS} is applied between the drain and the source and sets up a drain current (I_D) as shown. The gate-source voltage (V_{GS}), reverse biases the gate-source diode. Just as in a simple diode, the depletion region grows as the reverse bias across the pn junction is increased. This reduces the cross sectional area of the conducting n-channel, making it narrower, and thereby increasing the resistance and controlling the drain current I_D. Increasing V_{GS} will further constrict the channel and will cause I_D to drop.

As V_{GS} increases (becomes more negative) I_D decreases.

The JFET - Operation Overview

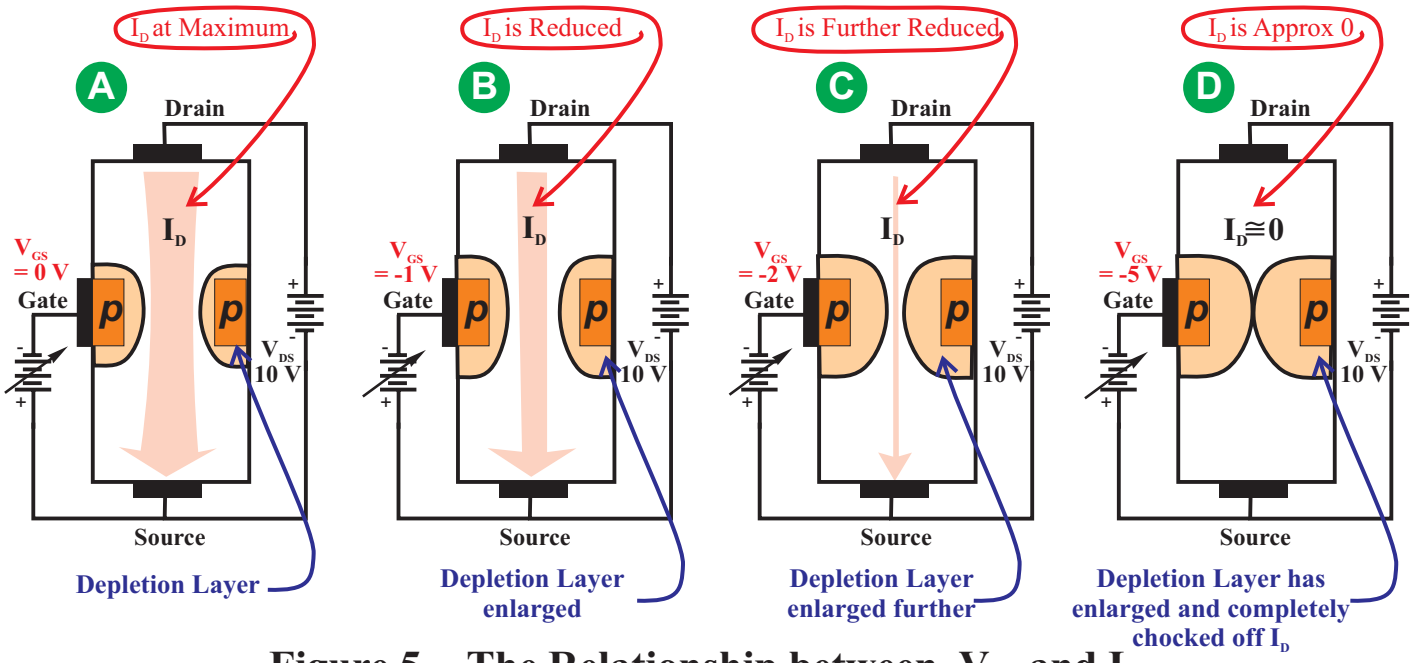


Figure 5 - The Relationship between V_{GS} and I_D

A V_{GS} is zero. The maximum drain current I_D is flowing.

B V_{GS} is increased to -1 V. This causes the depletion layer to enlarge into the channel. This reduces the size of the channel, which reduces I_D.

C V_{GS} is increased to -2 V. This causes the depletion layer to enlarge further into the channel which further reduces I_D.

D V_{GS} is increased to -5 V. This causes the depletion layer to enlarge and completely choke off the channel. This causes I_D to be reduced to near zero. The value of V_{GS} that causes I_D to be reduced to this near zero value is called **the gate-source cutoff voltage $V_{GS(off)}$**

Note : $V_{GS(off)}$ varies for different JFETS

Another Way to control I_D

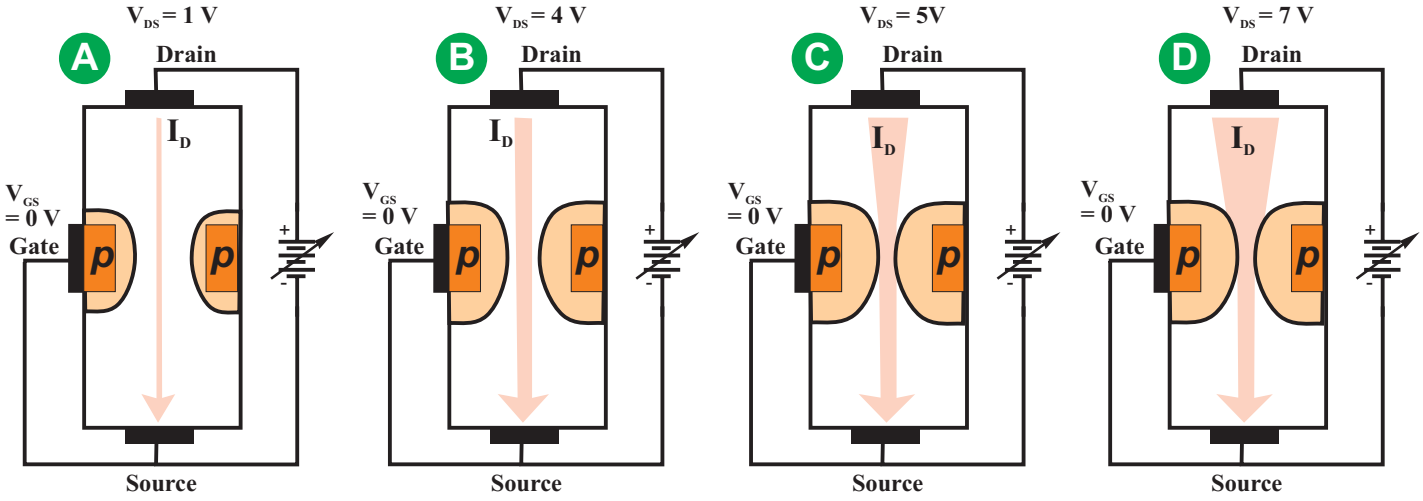


Figure 6 - The effects of varying V_{DS} with constant V_{GS}

A In Fig. 6 (A) V_{GS} is 0. A small depletion layer exists around the gate. The depletion layer exists because of the relationship between V_{GS} and V_{DS}. The gate (p-type) is more negative than the drain (n-type). This means that the pn junction between the gate and the n type channel is reverse biased and the depletion layer will grow as wide as necessary to reach equilibrium. This depletion layer extends into the channel and reduces its size.

B In Fig. 6 (B) V_{GS} remains at 0. Note that V_{DS} is now 4 V. This further increases the reverse bias on the gate diode. The depletion layer increases into the channel and reduces the current I_D. At the same time, increasing V_{DS} to 4 V increases the current I_D. Now we have two forces working against each other. Increasing V_{DS} will increase the current I_D while, at the same time, the depletion layer is increasing to reduce the current I_D. The forces are not yet equal. V_{DS} is the stronger force at this point, and I_D will increase to a new higher value.

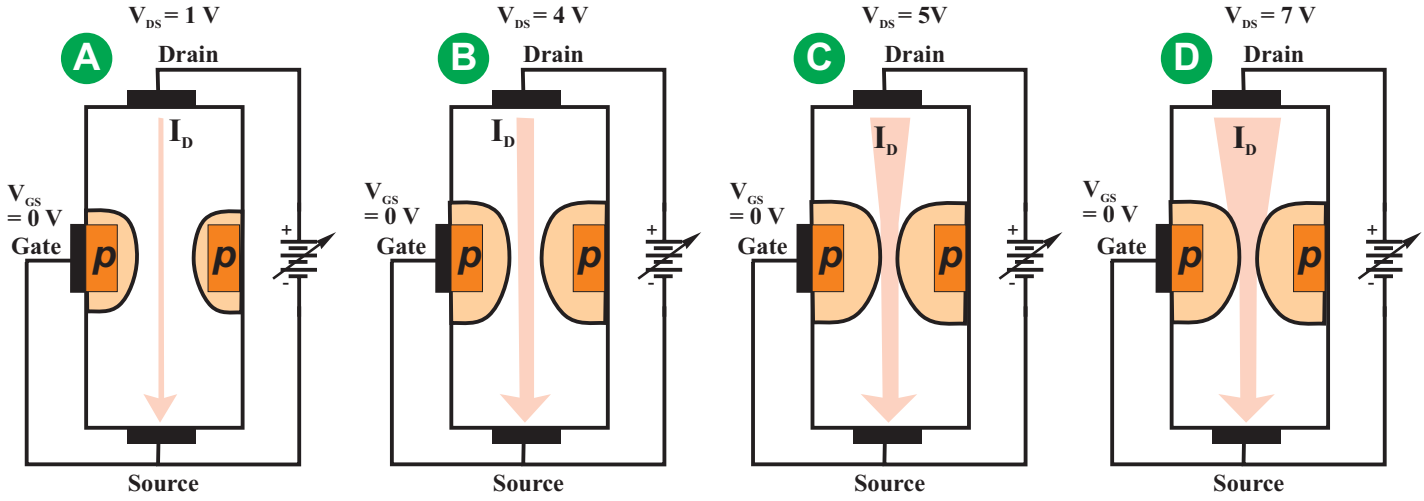


Figure 6 - The effects of varying V_{DS} with constant V_{GS}

C In Fig 6 (C) V_{GS} remains at 0. Note that V_{DS} is now 5 V. The two forces are now equal in magnitude. The value of V_{DS} at which this occurs is called the **Pinch-off voltage (V_P)**

D In Fig 6 (D) V_{GS} remains at 0. Note that V_{DS} is now 7 V. The two forces continue to be equal in magnitude. Increasing V_{DS} will try to increase I_D, but the enlarging of the depletion layer into the channel will resist the increase. I_D will remain relatively constant. Further increases in V_{DS} will not increase I_D.

Figure 7 shows the drain curve for the description above. The part of the curve to the left of V_P is called the ***ohmic region***. As V_{DS} increases from 0 to V_P, the drain current increases.

Here, the JFET is acting like a resistor, a linear increase in V_{DS} causes a linear increase in current I_D

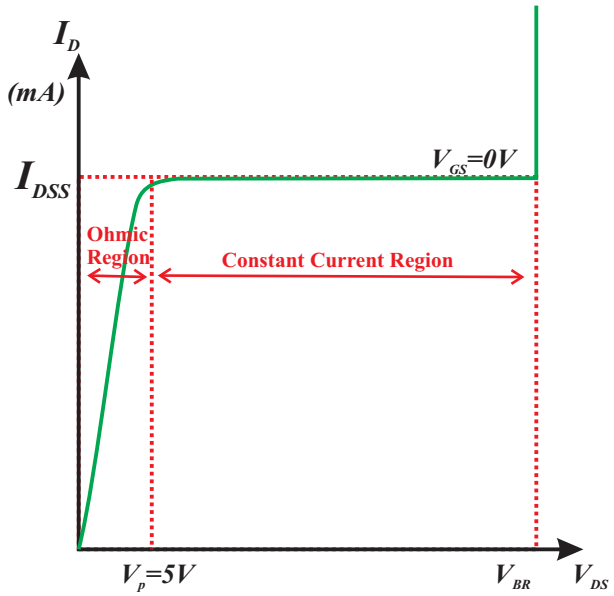


Figure 7 - Shorted Gate Drain Curve showing the constant-current region and the ohmic region

Constant- Current Region

As V_{DS} increases above the value of V_P, the value of drain current levels off at a relatively constant value.

The region of operation between V_P and V_{BR} is called the ***constant-current region.***

$\mathbf{V_{GS}}$ is the voltage measured from the ***gate to the source***.

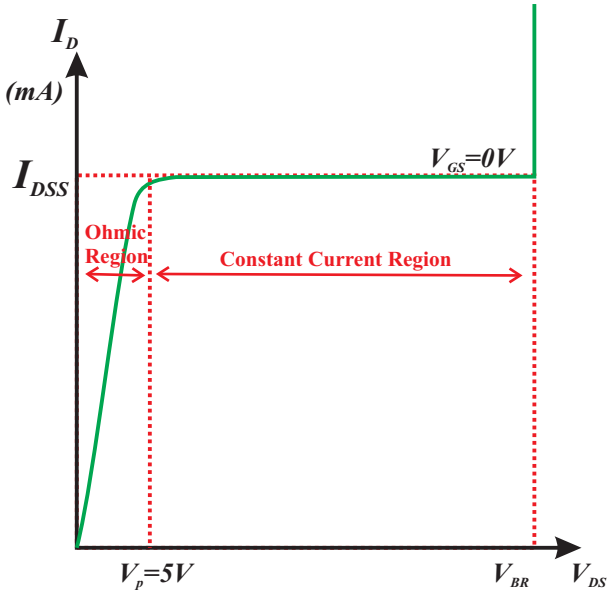


Figure 7 - Shorted Gate Drain Curve showing the constant-current region and the ohmic region

When $V_{GS} = 0$, the potential difference between the gate and the source is 0. We essentially have shorted the gate to the source. This guarantees that $V_{GS} = 0$.

When $V_{GS} = 0$, the drain current will be at its maximum possible value. This ***shorted gate drain current*** is called $\mathbf{I_{DSS}}$ and it is the maximum value of I_D.

The value of I_{DSS} is listed on the spec sheet and is measured under the following conditions:

$$\mathbf{V_{GS} = 0 \quad and \quad V_{DS} = V_P}$$

Any value of JFET drain current cannot be greater than I_{DSS}. I_{DSS} can be compared with $I_{C(sat)}$ in a BJT circuit. It is the maximum possible current that can flow in the drain circuit.

Drain Curves

Figure 8 shows the drain curves for $V_{GS} = 0$ through $V_{GS} = -5V$.

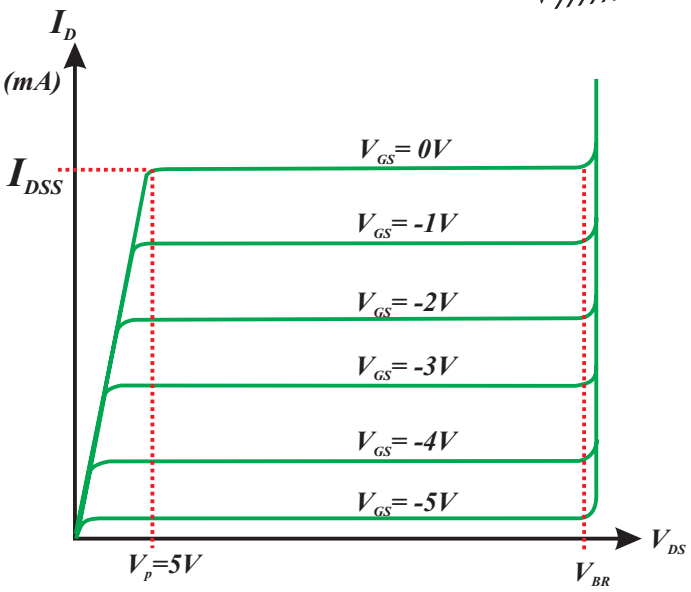


Figure 8 -- Normal Drain Curves

Note that as V_{GS} increases in a negative direction, the value of I_D decreases toward 0.

As V_{GS} becomes more and more negative, the point is reached where the channel becomes blocked off by the depletion layer. I_D is now approximately 0. In Figure 8, this happens when $V_{GS} = -5V$.

The value of V_{GS} that reduces I_D to this near 0 value is called the ***gate-source cutoff voltage*** **($V_{GS(off)}$)**

At $V_{GS(off)}$, current through the device stops.

For conduction to occur, the value of V_{GS} must be between $V_{GS} = 0$ and $V_{GS(off)}$

The Relationship between V_P and $V_{GS(off)}$

This relationship always exists:

$V_{GS(off)}$ & V_P ***will always have the same magnitude and opposite polarity.***

As an example: If V_P is 5 V , then $V_{GS(off)}$ will be -5V.

Since these two values are ***always*** equal magnitude and opposite polarity, only one will generally be listed on the device spec. sheet.

Definitions

Gate - source cutoff voltage $V_{GS(off)}$

The value of V_{GS} that reduces I_D to approx. 0.
For the JFET, $V_{GS(off)}$ is always equal in magnitude and has the opposite polarity as V_P.

Pinch-off Voltage V_P

The value of drain-source voltage (V_{DS}) that allows maximum JFET current (I_D) measured at $V_{GS} = 0$
For the JFET $V_P = -V_{GS(off)}$

Shorted gate-drain current I_{DSS}

The maximum possible value of I_D.

Ohmic Region

The portion of the JFET operating curve that lies below V_P.

Constant-current Region

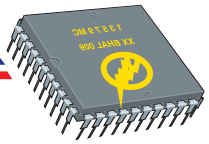
The portion of the JFET operating curve (between V_P and V_{BR}) where the drain current remains constant for fixed values of V_{GS}.

JFET Biasing

JFETs are always reverse biased. This means that the ***gate source junction is always reverse biased.***

In the explanation for Figure 6, we said that even when the gate is shorted to the source and $V_{GS} = 0$, the ***gate source junction is still reverse biased.***

We ***never allow the gate source junction to become forward biased*** because the junction is not designed to handle any significant current.



JFET Biasing

Since the gate is always reverse biased, the reverse current will be near zero. This means that JFETs have an extremely high gate input impedance that is typically in the high megohm range.

The data sheet for the MPF102 (the JFET that you have in your kit,) lists the maximum gate reverse current $\mathbf{I_{GSS}} = \mathbf{2\ nA}$ under the following conditions. $\mathbf{T = 25^oC}$ $\mathbf{V_{DS} = 0}$ $\mathbf{V_{GS} = -15V}$

Using Ohm's Law

$$\textbf{Gate Impedance} = \frac{|-15V|}{2\ nA} = 7.5\ G\Omega$$

The advantage of this extremely high input impedance is that it draws almost zero current from the source. This means that the JFET is almost no load on the source at all.

The JFET is heavily used in integrated circuits since it has such a low current requirements. It runs cool, and this is a big advantage in an IC where thousands of FETs are etched into one small piece of silicon.

The dc Biased JFET Circuit

We know that the JFET is a voltage controlled device ---- the output characteristics are controlled by the input or gate voltage.

We know that the size of the channel is controlled by the amount of reverse bias applied to the gate source-junction. This is what makes the device voltage controlled. It is the magnitude of V_{GS} that controls the drain current I_D.

For the BJT --- h_{FE} is a measure of how effectively the input current controls the output current.

For the JFET --- Transconductance is a measure of how effectively the input voltage controls the output current.

The output current (I_D) can be defined in terms of the circuit input voltage by the formula:

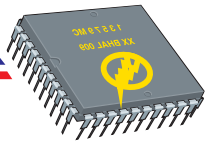
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

I_{DSS} = the shorted gate-drain current rating of the device
V_{GS} = the gate-source voltage
$V_{GS(off)}$ = the gate-source cutoff voltage

Note: ***The value of I_{DSS} and $V_{GS(off)}$ are component values and are constants for a given JFET.***

The value of V_{GS} is the only variable on the right side of the equation. This means that I_D is strictly a function of V_{GS} and if V_{GS} changes I_D will also change.

Ex. 12.1 demonstrates the use of the above equation



Plotting The Transconductance Curve

Plotting the transconductance curve for a specific JFET is a graph of all possible combinations of V_{GS} and I_D for a specific device.

The process for plotting the transconductance curve for a given JFET is as follows:

1. **Plot a point on the x- axis that corresponds to the value of $V_{GS(off)}$.**
2. **Plot a point on the y- axis that corresponds to the value of I_{GSS}.**
3. **Select 2 or 3 values of the V_{GS} between 0 V and $V_{GS(off)}$. For each value of V_{GS} selected, determine the corresponding values of I_D using the equation.**
4. **Plot the points from step 3, and connect all the plot points with a smoother curve.**

Ex. 12.2 shows this process

It is important to be able to plot the transconductance curves for the JFET.

These curves are used in both the dc and ac analyses of any amplifier using the JFET.

Most JFET spec. sheets list 2 values of $V_{GS(off)}$ and I_{DSS}. These are the maximum and minimum values.

When a range of values are given, we must use t***he two minimum values to plot one curve*** and the ***two maximum values to plot the second curve***.

The Maximum & Minimum Transconductance Curves

For the MPF102 in your kit the following values are given:

$V_{GS(off)} = -2\ V_{assumed}$ (min) $I_{DSS} = 2$ mA (min)

$V_{GS(off)} = -8$ V (max) $I_{DSS} = 20$ mA (max)

Using the procedure on the previous page, the maximum and minimum curve are plotted for the MPF102 in Figure 9.

Ex. 12.3 shows the complete process for finding the Max. & Min. Transconductance Curves.

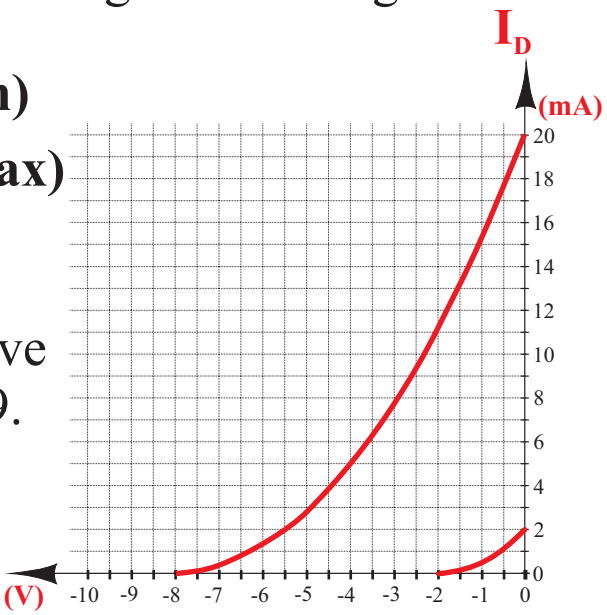


Figure 9 Transconductance curves
Max. & Min. curves for the MPF102

We have been working with the n-channel JFET in all examples. The n-channel JFET is much more commonly used than the p-channel JFET.

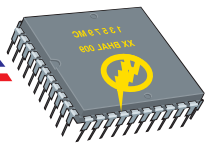
All of the principles for the n-channel JFET apply to the p-channel JFET. As with npn and pnp BJTs simply reverse the polarity of the voltages and currents.

Comparison of JFET and the BJT

Remember that:

The JFET is a voltage controlled device

The BJT is a current controlled device



The JFET - Operation Overview

Review of the dc Biased BJT

Keeping it very simple, we said earlier that if I_B is 10 μA in a BJT that has an h_{FE} of 100, then I_C will be 100 times I_B or 1 mA as shown in Figure 9(a).

$I_B = 10\ \mu A$
$I_C = h_{FE}I_B = 1mA$
$I_E = 1.01\ mA$

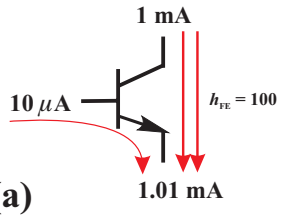


Figure 9(a)

$I_B = 20\ \mu A$
$I_C = h_{FE}I_B = 2\ mA$
$I_E = 2.02\ mA$

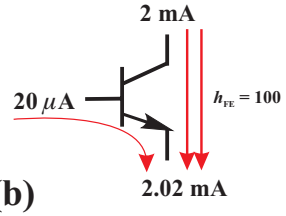


Figure 9(b)

$I_B = 50\ \mu A$
$I_C = h_{FE}I_B = 5\ mA$
$I_E = 5.05\ mA$

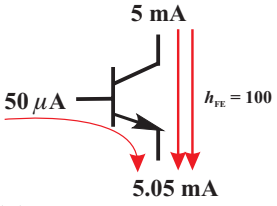


Figure 9(c)

If we assume a linear relationship between I_B and I_C, then Figure 9(b) and 9(c) are also true.

If we were to graph this simple relationship shown above, we would get the graph in Figure 10.

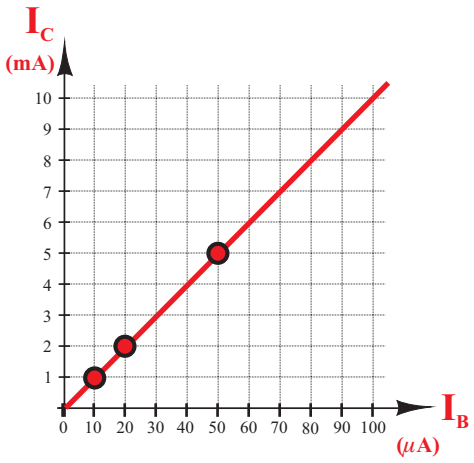


Figure 10 BJT I_C vs I_B

This relationship would continue until the transistor becomes saturated. At that point, further increases in I_B will not increase I_C.

In reality, the relationship is not totally linear.

Figure 11 shows a more typical curve. Note that there is some non-linearity in the curve which can cause some distortion in the output. Remember that for the BJT:

- the output current I_C is controlled by the input current I_B

The BJT is a current controlled device

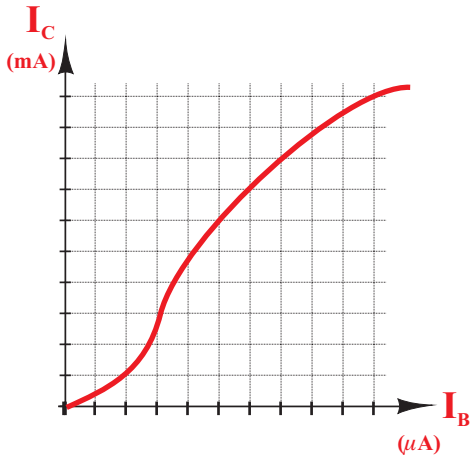


Figure 11 A more typical BJT I_C vs I_B

Review of the dc Biased BJT

There is a reason that we are doing all this. We are about to examine the relationship between the input and output side of the BJT.

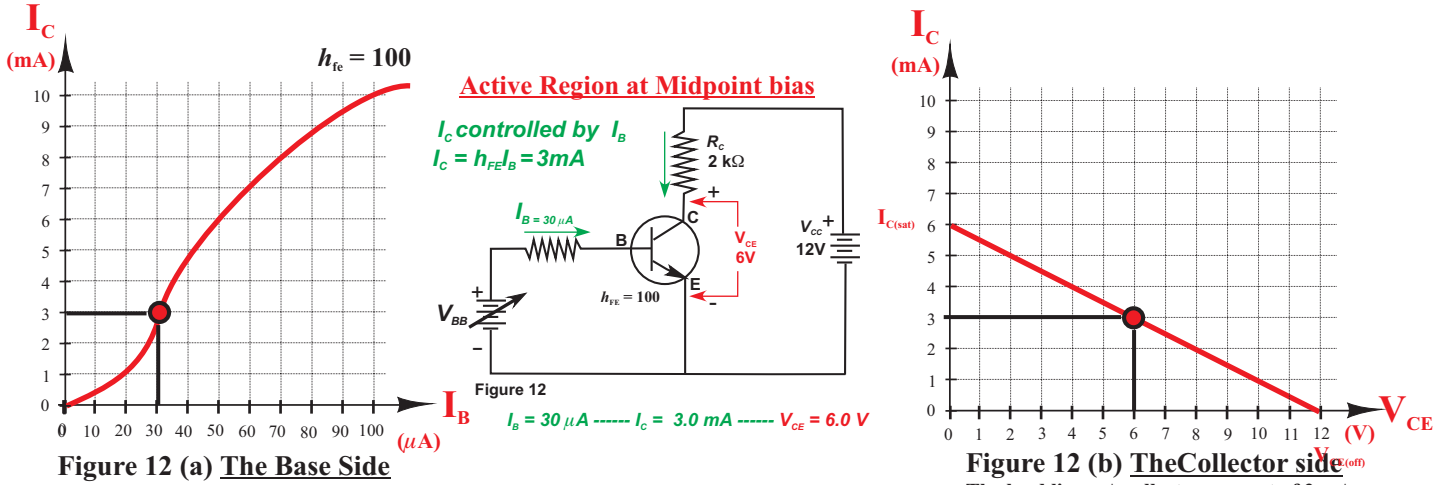


Figure 12 (a) The Base Side
A base current of 30 μA produces a collector current of 3 mA

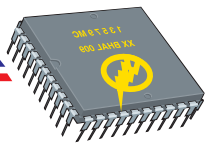
Figure 12 (b) TheCollector side
The load line – A collector current of 3 mA produces a Q point at midpoint bias

Figure 12 (a) shows the comparison of base current versus collector current. Note that a 30 μA base current produces a 3 mA collector current when h_{FE} is 100.

Figure 12 (b) shows what is going on in the collector circuit. The 3 mA collector current produces a Q point in the middle of the load line and V_{CE} is 6V.

Note that the output characteristics are controlled by the input current.

Now we will use the same type of analogy using the MPF-102 JFET that you have in your kit.



Active Region at Midpoint bias

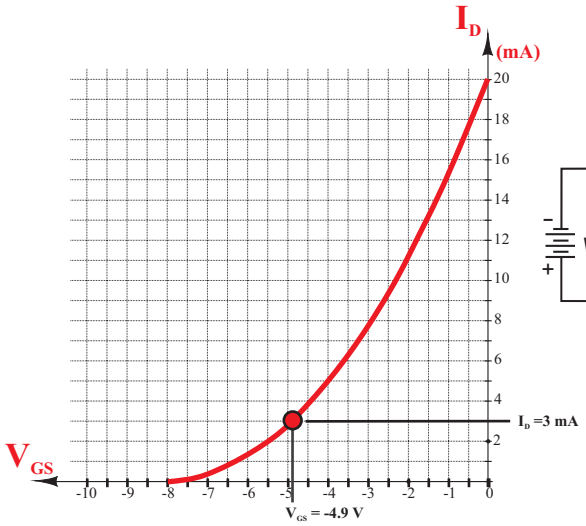


Figure 13 (a) The Gate Side
A V_{GS} of -4.9V produces a drain current of 3 mA This particular JFET has :

$V_{GS(off)}$ = -8 V
I_{DSS} = 20 mA

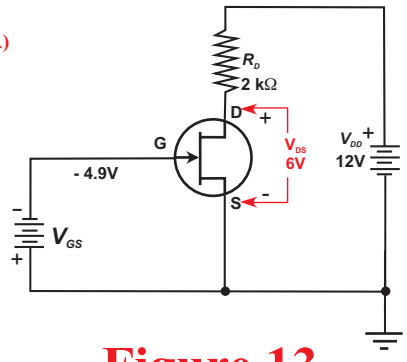


Figure 13

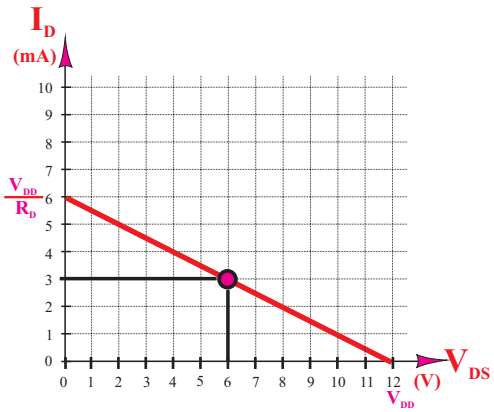


Figure 13 (b) The Drain Side
The load line – A drain current of 3 mA produces a Q point at midpoint bias

By Calculation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 20\text{mA}\left(1 - \frac{-4.9\text{ V}}{-8\text{ V}}\right)^2$$

$$= 20\text{mA}\left(1 - 0.6125\right)^2$$

$$= 3.003\text{ mA}$$

The Gate Side

Figure 13 (a) shows an MPF 102 that has a $V_{GS(off)}$ of -8V and an I_{DSS} of 20 mA. The transconductance curve has been plotted and appears in Fig. 13 (a). This curve is a comparison of V_{GS} to I_D. Note that, for this particular JFET, a V_{GS} of -4.9V will produce a drain current of 3 mA. Note that the transconductance curve is not linear. We will see later that this can cause distortion at the output when an ac signal is applied.

The Drain Side

Figure 13 (b) shows the load line for this circuit. It is very similar to the load line for the BJT. Ideally, we want the Q point in the centre of the load line, but we will find that this can be somewhat difficult to achieve.

Biasing Methods

For the JFET, we are going to study four different biasing methods - ***Gate Bias, Self Bias, Voltage Divider Bias*** and ***Current Source Bias***. We will see that each method gets progressively better at controlling the Q point of the device.

Controlling the Q Point

The manufacturing spread for JFETs is much worse than they are for bipolar transistors. For this reason, the Q point can be much harder to control with the JFET.

With the 2N3904 junction transistor, we saw a beta range of between 100 and 300.This is a 3 to 1 spread in range.

With the MPF102 JFET we have a I_{DSS} range of 2mA to 20 mA. This is a 10 to 1 spread in range.

This large range of values of I_{DSS} from device to device is what makes the Q point hard to control.

Gate Bias

Gate bias is the JFET counterpart to base bias with the BJT. A gate bias circuit is shown in Figure 14.

The gate supply voltage (V_{GG}) is used to ensure that the gate source junction is reversed biased.

Since there is no gate current, there is no voltage dropped across R_G, and the value of V_{GS} is found as $\mathbf{V_{GS} = - V_{GG}}$

V_{DS} (similar to V_{CE} in base bias) is found as: $\mathbf{V_{DS} = V_{DD} - I_D R_D}$

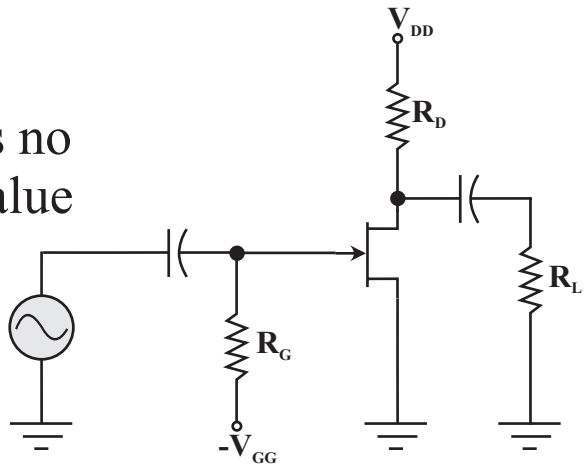


Figure 14 Gate Bias

Examples 12.4 and 12.5 explain gate bias. It is very important that you understand both of these examples.

Why do we need the resistor R_G

We said previously, that the there is no gate current through R_G. Since resistors are usually used to drop a voltage, then why do we need it?

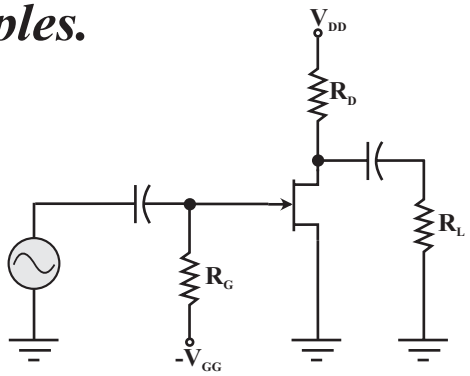


Figure 15(a) Why we need R_G

Figure 15 (b) shows R_G removed and replaced with a wire. Now any ac signal from the generator is shorted to ground through the dc source V_{GG}. The resistor allows the ac develop across it, making it appear at the gate of the FET.

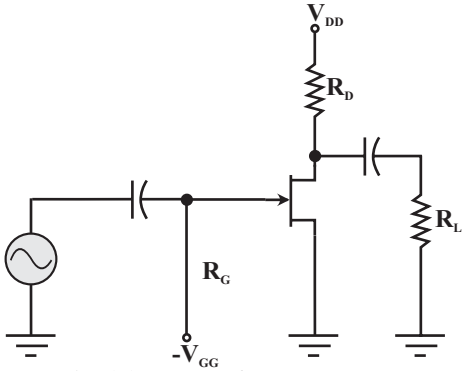


Figure 15 (b) Removing R_G shorts the ac to ground through V_{GG}

Self Bias

Self Bias is one of the more popular methods of biasing the JFET.

Note that R_G now goes to ground.

Note also that R_S has been added.
Rs helps to produce the $-V_{GS}$ required to bias the JFET.

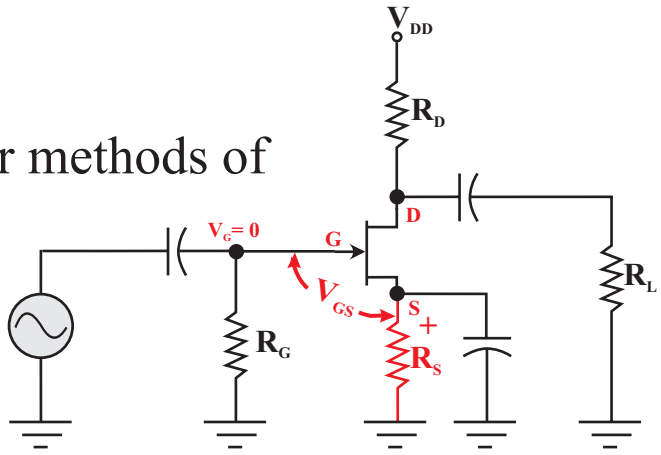


Figure 16 Self Bias

In this circuit, the drain current and the source current are the same since all of the drain current passes through the channel and leaves via the source.

$$I_S = I_D$$

This drain current all also passes through R_S and a voltage drop will appear across it.

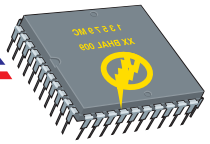
$$V_S = I_D R_S$$

Note that V_{GS} is the potential measured from the gate (+) to the source (-). The gate is at zero volts since it is at ground potential rough R_G. Remember that there is no gate current. Since the source end is at a positive potential ($V_S = I_D R_S$), then V_{GS} is defined by:

$$V_{GS} = -I_D R_S$$

The negative V_{GS} is developed by the current through the source resistor.

Example 12.6 and 12-7 are an example of Self Bias Calculations.



Self Bias - Rules for Plotting the Bias Line

To plot the dc bias line for self bias , follow this procedure:

1. Plot the minimum and the maximum transconductance curves for the JFET used in the circuit.

2. Choose any value of V_{GS} and determine the corresponding value of I_D using the formula: $$I_D = \frac{-V_{GS}}{R_S}$$

3. Plot the point determined above and draw a line from this point to the origin of the graph.

4. The points where the line crosses the two transconductance curves defines the limits of the Q point for any of this type of JFET used in the circuit.

The JFET - Biasing Methods