Lab 4 Small Signal CE Amplifiers

Name _____ **Section** _____

Purpose:

* To demonstrate the ac operation of the common emitter CE amplifier.
* To demonstrate the effect of the bypass capacitor on amplifier gain (A_V)
* To calculate the loaded and unloaded gain of the amplifier.

Equipment:

* 1 dc Power Supply
* 1 Digital Multimeter (DMM)
* 1 Variable ac Signal Generator **(40 mV_{p-p} output)**
* 1 Dual Trace Oscilloscope
* 1 2N3904 npn transistor
* 6 Resistors 1 - 330 Ω 1 - 10 kΩ
* 2 10 μF Capacitors 1 - 1 kΩ 1 - 3.3 kΩ
* 1 100 μF Capacitor 1 - 2 kΩ

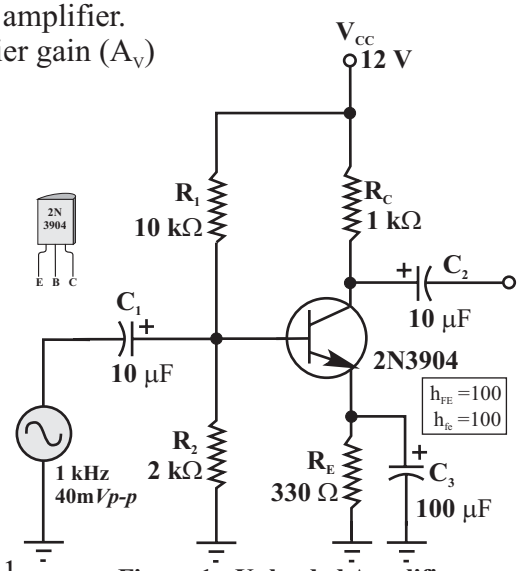


Figure 1 - Unloaded Amplifier

Pre-Lab Preparation *See Page 5*

Calculate the "unloaded"or "no load" voltage gain for Figure 1
Calculate the "loaded" voltage gain for Figure 2
Calculate the "loaded" voltage gain with the bypass capacitor removed in Figure 3

Discussion:

The input signal to a CE amplifier is applied across the emitter- base junction of our transistor. The output signal is taken from the collector terminal of the transistor.

The CE amplifier is one of the most commonly used BJT amplifier configurations. This amplifier has a relatively high voltage gain and a voltage phase shift of 180^{O} from base to collector. (input to output).

In this lab, we will observe the ac operation of the CE amplifier. We will also observe the effects of the emitter bypass capacitor. Remember that the purpose of this capacitor is to hold the emitter of the transistor at ac ground. This action increases the voltage gain of the CE amplifier.

Procedure: (A) No Load

1) Construct the circuit shown in Figure 1. Note that R_L is not in the circuit.

2) Turn on the power supply. This circuit <u>should</u> be midpoint biased. Is it.? (yes/no) _____
What is the value of V_{CE} _____

3) Hook up the signal generator to the input of the circuit. Set the generator to produce a 1 kHz, 40 mV_{p-p} signal. **Be sure to connect the signal generator to the circuit before you set the output level to 40 mV_{p-p} The circuit is the load for the generator and it will slightly reduce the output level when it is connected to the generator. Setting the output level after the circuit is connected is the more accurate way to do this.**

4) Measure and record the peak-to-peak input & output voltage of the amplifier

V_{in} = _____ V_{out} = _____

5) Using V_{in} and V_{out}, calculate the ordinary voltage gain of the amplifier. A_V _____
Show your calculation

Lab 4 Small Signal CE Amplifiers

Procedure (B) 3.3 kΩ load

1) Add the 3.3 kΩ load resistor as shown in Fig. 2.
Reset the input signal level to 1kHz at 40 mV$_{p-p}$

2) Measure and record the peak-to-peak output voltage at the collector terminal of the transistor.

V_{in} = _____ V_{out} = _____

3) Using V_{in} and V_{out}, calculate the ordinary voltage gain of the amplifier. A_V _____
Show your calculation

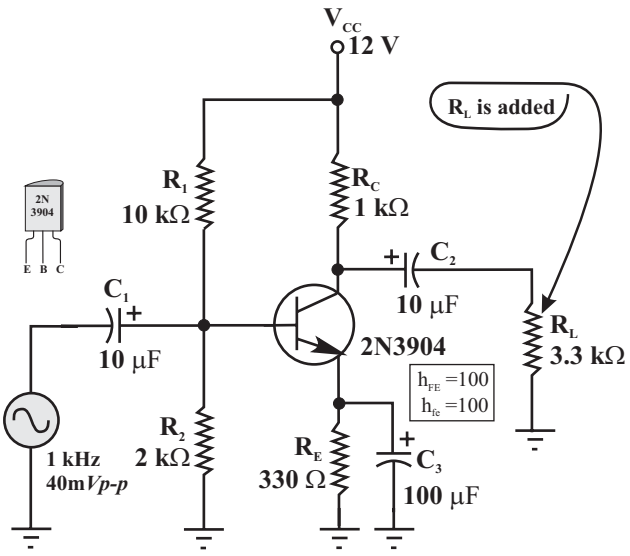


Figure 2 - Loaded amplifier with 3.3 kΩ load

Coupling Capacitors

1) The coupling capacitors in an amplifier are used to block dc while allowing the ac signal to pass. Look at C_2. Using the oscilloscope, measured the ac peak-to-peak voltage on both sides of the capacitor and record it below.

V_{p-p} _____ on the load side of C_2.
V_{p-p} _____ on the transistor side of C_2.

2) Now using the DMM, measured the dc voltage on both sides of C_2, and record it below.

V_{dc} _____ on the load side of C_2
V_{dc} _____ on the transistor side of C_2.

3) Do your measurements support the statement that the coupling capacitor passes ac while blocking dc?
_____

Phase Shift

1) We know that the CE amplifier produces a voltage phase shift of 180° from base to collector **(input to output).**

-Using the oscilloscope, connect *Channel 1* to the base and *Channel 2* to the collector of the transistor

-Adjust the vertical sensitivity of each channel so that each signal amplitude fills less than half of the screen's total height.

-Adjust the vertical position of the signals so that the input signal is in the upper half of the screen, while the output signal is in lower half of the screen.

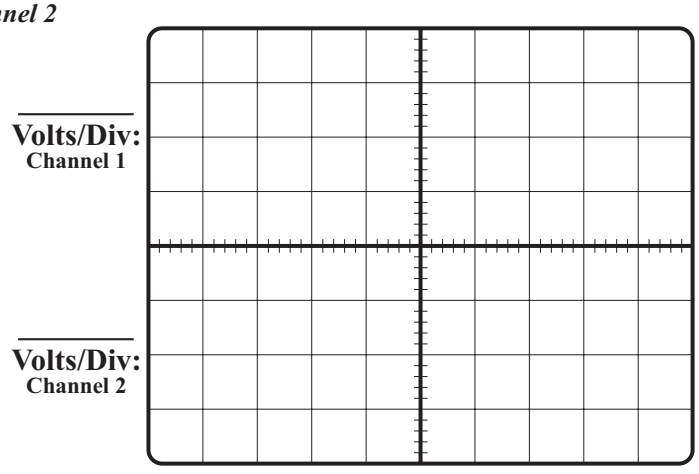
-Adjust the time-base so that approximately two complete cycles are shown on the screen.

-Be sure to set the *vertical mode switch to chop*

-Neatly draw the waveforms shown on the scope on the grid.

-Label the input and the output.

-Fill in Time/Div and V/Div in the space provided.



Time/Div: _____

Lab 4 Small Signal CE Amplifiers

Procedure (C) (Remove Emitter Capacitor)

1) Remove the emitter bypass capacitor and shown in Figure 3.

2) Hook up the signal generator to the input of the circuit. ***Reset the input signal level to 1 kHz, at 40 mV*** $_{p\text{-}p}$

3) Measure and record the peak-to-peak output voltage across the load.

4) Calculate the voltage gain..***Show your calculation.***

V_{in} = _____

V_{out} = _____

A_V = _____

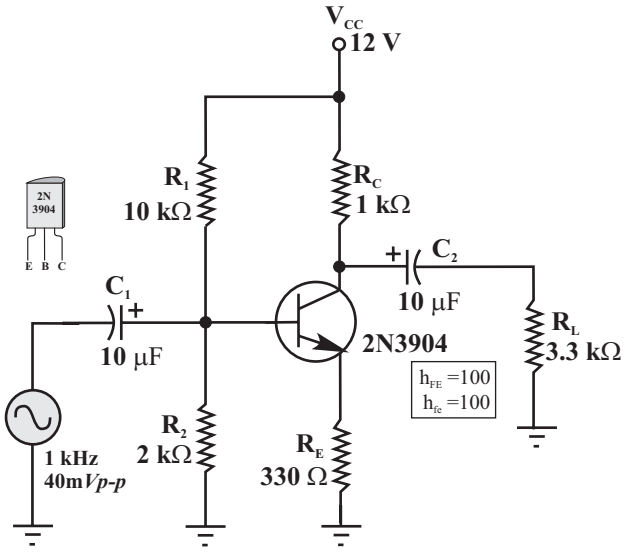


Figure 3 - Loaded amplifier with bypass capacitor removed

Questions

Procedure: (A) No Load

1) In the pre-lab section, you calculated the unloaded gain for the circuit shown in Figure 1. In procedure (A), you calculated the voltage gain from the measured values. Compare these two values of A_V.

A_V_____ (Calculated from the schematic values **(pre-lab)**)
A_V_____ (Calculated from the measured values **(procedure (A))**
The ***most accurate voltage gain*** is (Calculated from the measured values **(procedure (A))** value above.

Give 3 reasons why this is true.

Procedure: (B) 3.3kΩ Load

1) In the pre-lab section, you calculated the loaded gain for the circuit shown in Figure . In procedure (B), you calculated the voltage gain from the measured values. Compare these two values of A_V.

A_V_____ (Calculated from the schematic values **(pre-lab)**)
A_V_____ (Calculated from the measured values **(procedure (B))**
The ***most accurate voltage gain*** is (Calculated from the measured values **(procedure (B))** value above.

– Why are the loaded gains above, lower than the unloaded gains in Procedure(A)

Questions (cont.)

Procedure: (B) 1kΩ Load (cont)

Coupling Capacitors

1) In the procedure (B) section , you measured and compared the ***ac signal*** that appears on both sides of capacitor C_2.

   (i) Does the capacitor appear to **pass** or **block** the ac signal ? _____

2) In the procedure (B) section , you measured and compared the ***dc signal*** that appears on both sides of capacitor C_2.

   (i) Does the capacitor appear to **pass** or **block** the dc signal ? _____

3) Why are capacitors needed in the circuit ?

Phase Shift

1) In the procedure (B) section , you sketched the ac signal that appears at the input and output of the amplifier. The output should be 180^{O} out of phase with the input ?

   (i) Why is the output 180^{O} out of phase with the input ?

Procedure: (C) Remove Emitter Capacitor

1) In the pre-lab section, you calculated the loaded and swamped gain for the circuit shown in Figure 3. In procedure (C), you calculated the voltage gain from the measured values. Compare these two values of A_V.

A_V_____ (Calculated from the schematic values **(pre-lab)**)
A_V_____ (Calculated from the measured values **(procedure (C))**

As before, the ***most accurate voltage gain*** is (Calculated from the measured values **(procedure (C))** value above. The two values above should be close to the same value.

(i) Give the main reason why these values above are near the same value

Lab 4 Small Signal CE Amplifiers

Pre-Lab ***(Complete all of this page)***

In Figure 1, to the right, the amplifier is operating "unloaded" since there is no load resistor on the amplifier.

The unloaded gain is found as $A_V = \frac{R_C}{r'_e}$

Calculate the unloaded gain for Figure 1.
Be sure to include R_{base} in your calculation.

A_V = _____

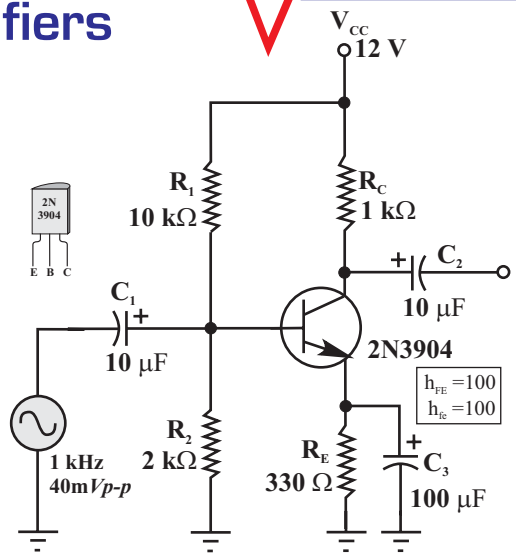


Figure 1 - Unloaded Amplifier

In Figure 2, to the right, the amplifier is operating "loaded" since there is a load resistor on the amplifier.

The loaded gain is found as $A_V = \frac{r_c}{r'_e}$ where $r_C = R_C || R_L$

Calculate the loaded gain for Figure 2.

A_V = _____

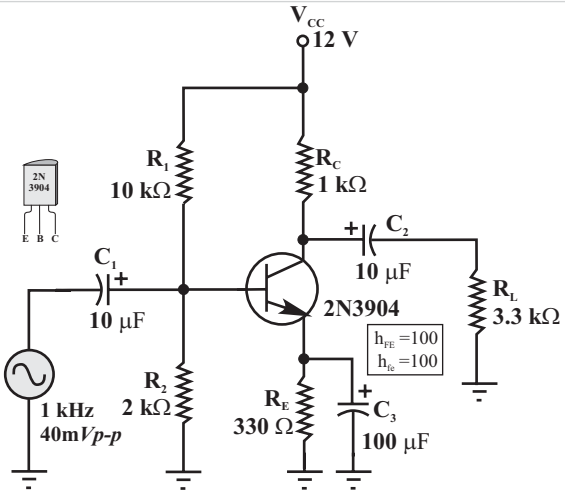


Figure 2 - Loaded amplifier with 3.3kΩ load

In Figure 3, the amplifier is operating "loaded" and swamped. The bypass capacitor has been removed, which exposes the 330Ω resistor (R_E) to the ac signal. This resistance must now be included in the gain equation. We now call it r_E since it now an ac value.

The swamped gain is found as $A_V = \frac{r_C}{r'_e + r_E}$ where $r_C = R_C || R_L$

Calculate the swamped gain for Figure 3.

A_V = _____

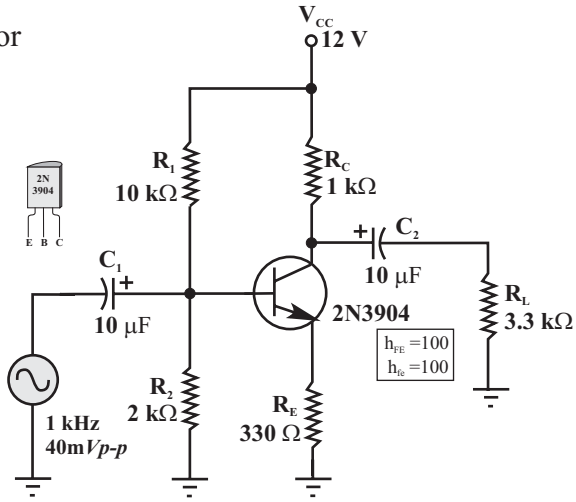


Figure 3 - Loaded amplifier with bypass capacitor removed