Lab 10 JFET Bias

Name _____ **Section** _____

For this Lab -- Please work is pairs. You require 3 MPF102 JFETs. Your kit supplies only 2.

Purpose:

* To examine four different bias methods for the JFET
* To examine the stability of each of these bias methods

Equipment

* 1 Agelent dc Power Supply and 1 bipolar power supply
* 1 Digital Multimeter (DMM)
* 1 2N3904 npn Transistor
* 3 MPF102 JFETs
* 9 Resistors
  - 1 -470 Ω
  - 1 - 680 Ω
  - 1 - 1 k Ω
  - 1 - 2.2 k Ω
  - 2 - 6.8 k Ω
  - 2 - 33 k Ω
  - 1 - 100 k Ω

Discussion

We know that controlling the Q point of our JFET is more difficult than it was with our junction transistor. This is because I_{DSS} varies widely from one JFET to the next. In order to stabilize I_D to a constant level from one JFET to another, we need a circuit that will vary V_{GS} widely.

Gate bias is the simplest but worst way to control the drain current. With gate bias, we supply a constant value of V_{GS} , and the resulting drain current will vary widely from device to device.

Self bias offers some improvement because the source resistor produces local feedback. Here, the value of V_{GS} varies somewhat with the value of drain current. This helps to control the drain current.

Voltage Divider bias results in a relatively stable Q point, however it requires a large supply voltage.

Current Source bias can produce the most stable Q-point because the bipolar transistor forces the drain current to a pre-determined value.

In this lab, we will calculate and draw the bias line of each of the four circuits. We will then predict the upper and lower limits of I_D from the bias line.

We will build each of the four biasing circuits and measure the performance of three JFETS in each circuit. We will compare the range of I_D as we progress through all 4 circuits. We will begin with Gate bias, then move on to Self bias, Voltage divider bias, and finally Current Source bias. Each of these circuits is described in detail in the notes. We should find that as we progress through each circuit, the measured range of I_D diminishes. In our Current Source Bias circuit, we should not only find that the I_D is very stable from JFET to JFET, but also that the value of I_D is very close to the value we predicted in our calculations.

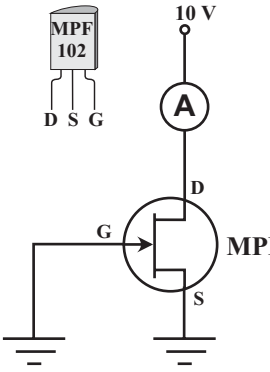
Prelab

Each biasing circuit has prelab section. Be sure to perform the calculations, draw the bias line and predict the range of I_D for each circuit. ***The prelab is on pages 4 and 5 of this lab.***

Lab 10 JFET Bias

Procedure (Complete pages 2 and 3 in the lab)

Measuring I_{DSS}



Measuring I_{DSS}
Figure 1

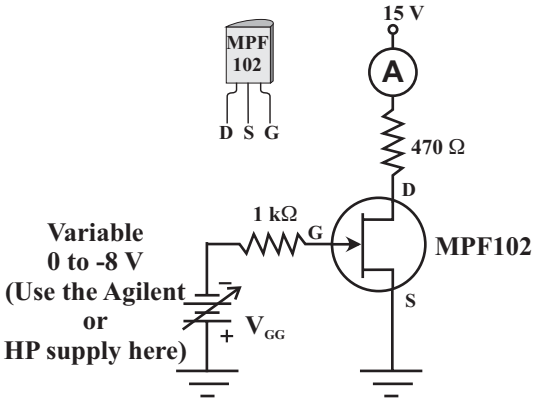
1) Refer to the data sheet included in this lab for the MPF-102. Notice that $V_{GS(off)}$ has a maximum of -8 V; the minimum value is not specified.
We will assume a minimum value of -2V for $V_{GS(off)}$
Also notice that I_{DSS} has a minimum value of 2 mA and the maximum value of 20 mA.

2) Connect the circuit shown in Figure 1. Measure the drain current.
Record this value of I_{DSS} in Table 1.
Note: Because of heating effects, the drain current may decrease slowly. Take your reading as soon after power-up as possible.

3) Repeat step 2 for the other 2 JFETs.

Table 1 I_{DSS} & $V_{GS(off)}$	I_{DSS}	$V_{GS(off)}$
JFET MPF102 (1)		
JFET MPF102 (2)		
JFET MPF102 (3)		

Measuring $V_{GS(off)}$



Measuring $V_{GS(off)}$
Figure 2

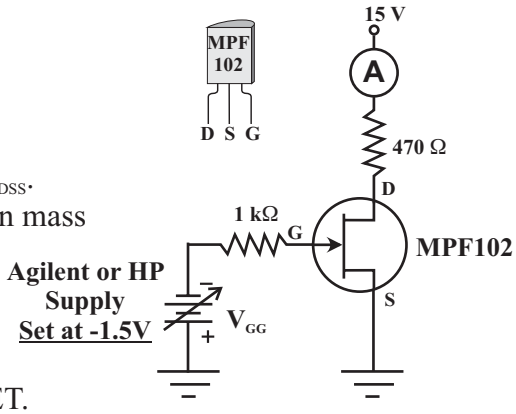
1) Figure 2 shows an approximate way of measuring $V_{GS(off)}$.
Build the circuit shown in Figure 2 . Insert the first JFET MPF102 (1) into the circuit.
Use the Agilent or HP power supply to supply V_{GS}. Use the digital meter that is part of the supply to measure the value of V_{GS}

2) Increase the negative gate supply voltage until the drain current drops to approximately 1 μA.
Record the value of $V_{GS(off)}$ in Table 1 above.

3) Repeat Step 1 & 2 for each of the other JFETs.

Gate Bias

1) With gate bias, you apply a fixed gate voltage that reverse biases the gate of the JFET. This produces a drain current that is less than I_{DSS}.
The problem is that you cannot accurately predict the drain current in mass production because of the variation in the required V_{GS}.
The following will illustrate this point.



Gate Bias
Figure 3

2) Build the circuit shown in Figure 3. Apply a V_{GS} of -1.5V.
Measure V_{GS}, I_D, and V_{DS}. and record the data in Table 2 for each JFET.

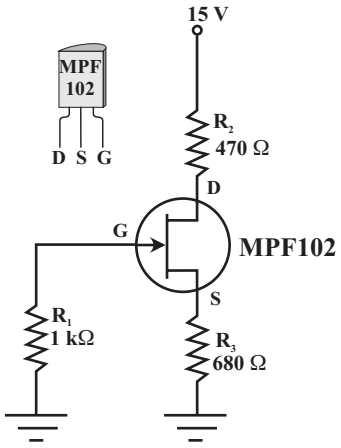
Table 2 Gate Bias	V_{GS}	I_D	V_{DS}
JFET MPF102 (1)	-1.5 V		
JFET MPF102 (2)	-1.5 V		
JFET MPF102 (3)	-1.5 V		

Lab 10 JFET Bias

Self Bias

1) Build the circuit shown in Figure 4. Measure and record the 3 values shown in Table 3. Repeat the measurements for the other JFETs.
The drain current variation for the self- bias circuit should be less than the variation than the gate-biased circuit.

Table 3 Self Bias	V_{GS}	I_D	V_{DS}
JFET MPF102 (1)			
JFET MPF102 (2)			
JFET MPF102 (3)			



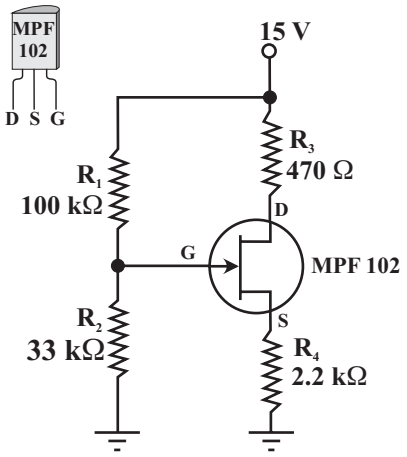
Self Bias
Figure 4

Voltage Divider Bias

1) Build the circuit shown in Figure 5. Measure and record the 3 values shown in Table 4. Repeat the measurements for the other JFET.

The drain current variation for the voltage divider bias circuit should continue to become more stable. It should show less variation than either of the circuits above.

Table 4 Voltage Divider Bias	V_{GS}	I_D	V_{DS}
JFET MPF102 (1)			
JFET MPF102 (2)			
JFET MPF102 (3)			



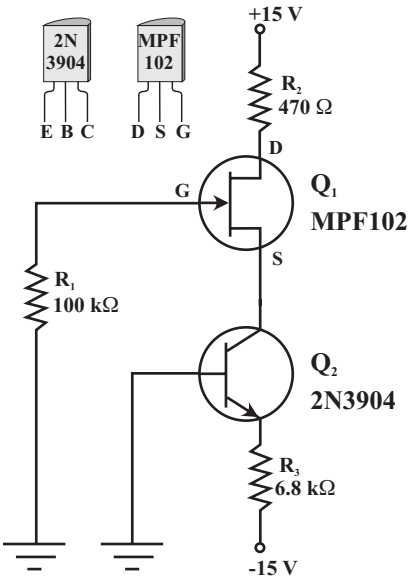
Voltage Divider Bias
Figure 5

Current Source Bias

1) Build the circuit shown in Figure 6. Measure and record the 3 values shown in Table 5. Repeat the measurements for the other JFET.

The drain current for the current source bias circuit should have less variation than any of the other circuits.

Table 5 Current Source Bias	V_{GS}	I_D	V_{DS}
JFET MPF102 (1)			
JFET MPF102 (2)			
JFET MPF102 (3)			



Current Source Bias
Figure 6

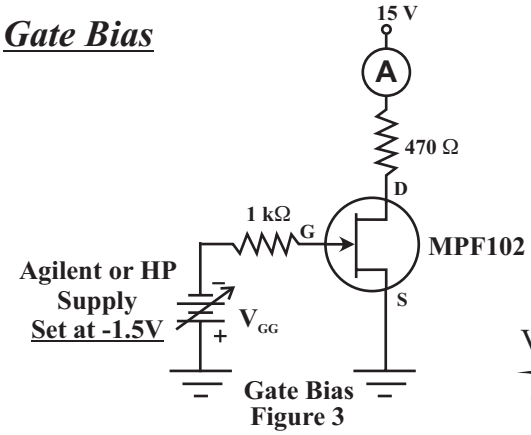
Lab 10 JFET Bias

Prelab Section *Drawing the Bias Lines and Predicting the Range of I_D*

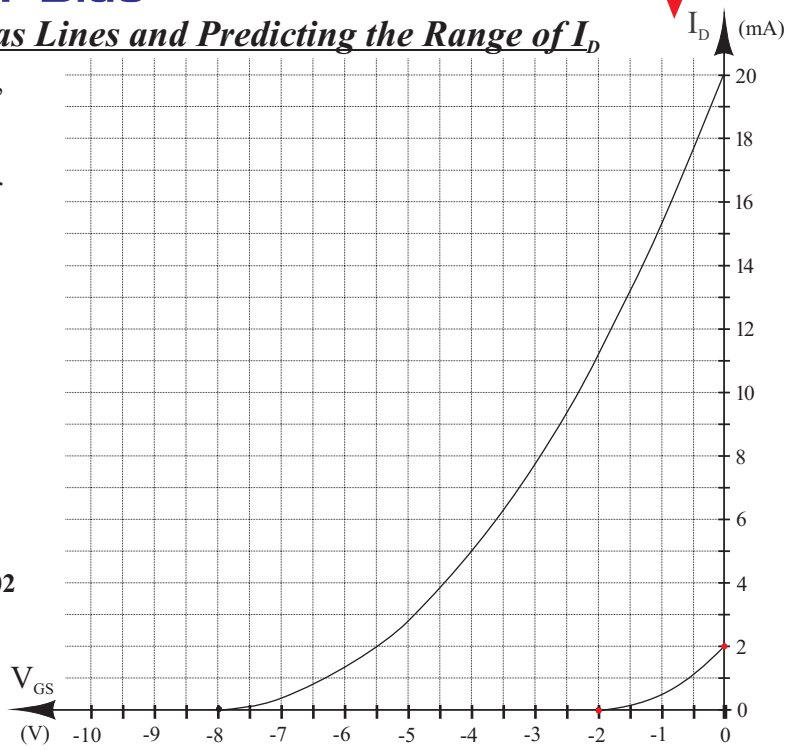
1) For each of the 4 bias circuits below, calculate and draw the bias line.

2) From the graph, determine the upper and lower values of drain current I_D. ***Enter your values in the predicted (prelab) portion of Table 6.***

Gate Bias

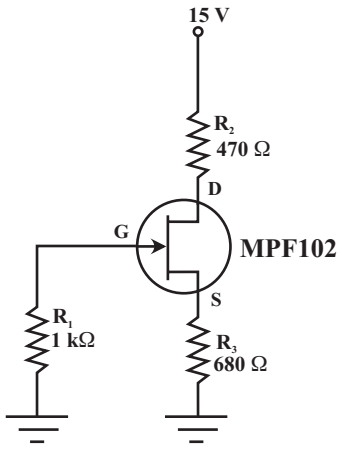


Gate Bias
Figure 3

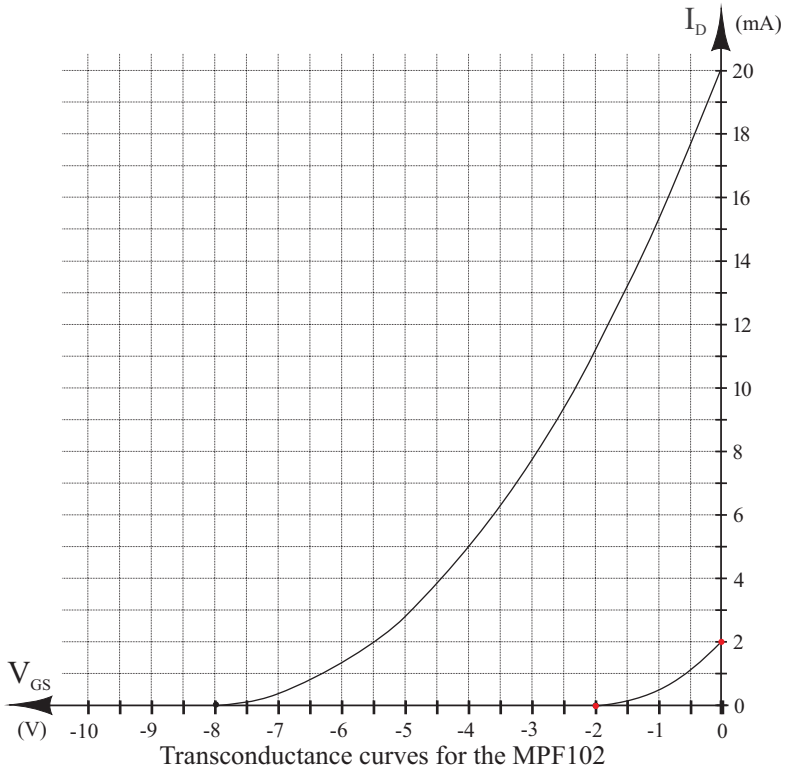


Transconductance curves for the MPF102

Self Bias



Self Bias
Figure 4



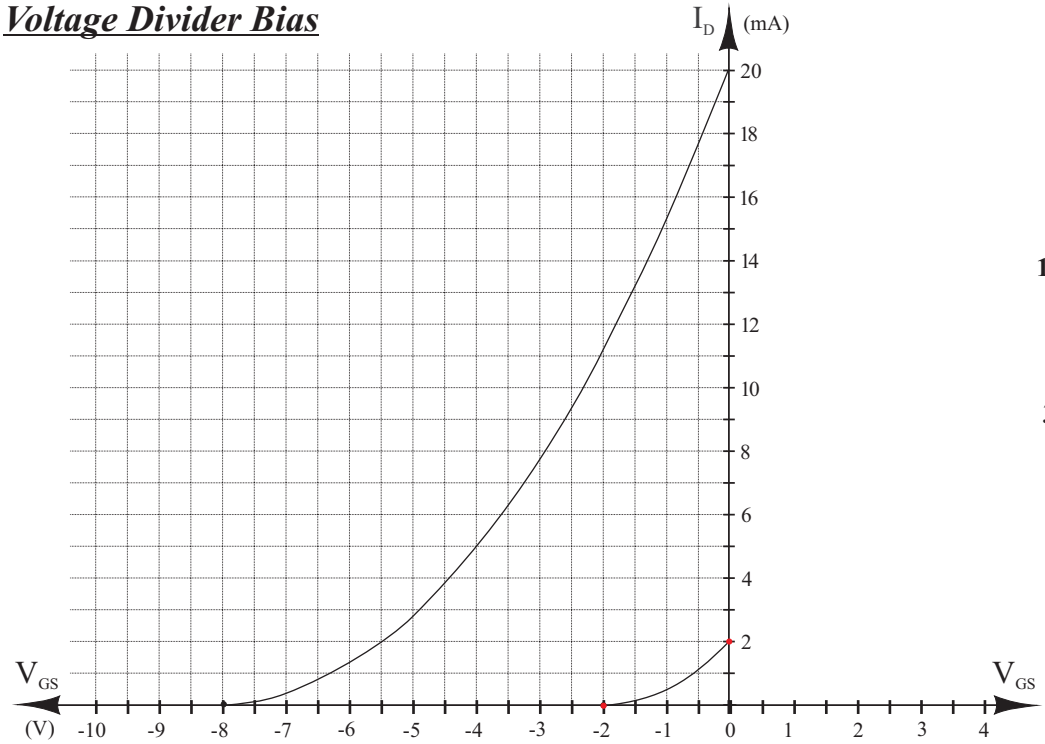
Transconductance curves for the MPF102

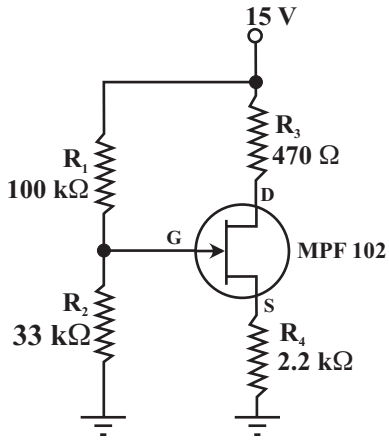
Show all calculations

Lab 10 JFET Bias

Prelab Section *Drawing the Bias Lines and Predicting the Range of I_D*

Voltage Divider Bias

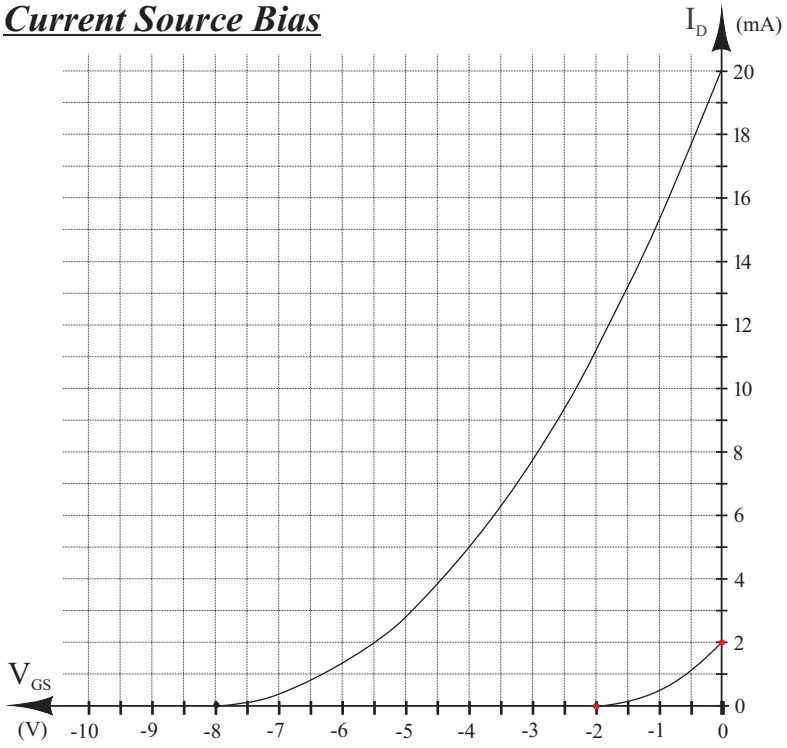


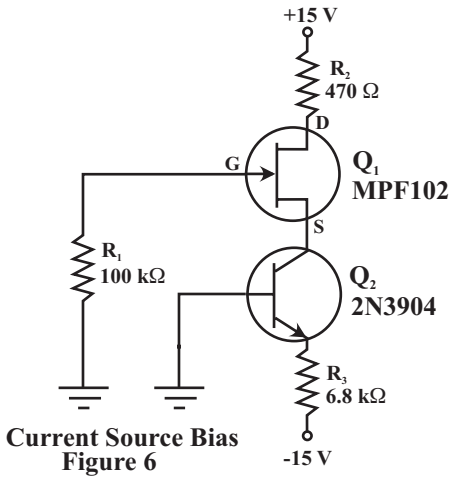


Voltage Divider Bias
Figure 5

Show all calculations

Current Source Bias





Current Source Bias
Figure 6

Show all calculations

Lab 10 JFET Bias

Questions

1) Look back at Tables 2 thru 5.

   For each bias type, note the minimum and maximum drain current that you measured.

   Insert the lowest and the highest measured value of I_D in the measured portion of Table 6.

Table 6

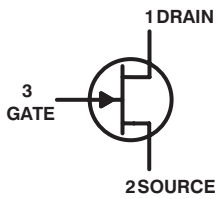
Bias Type Comparison	Predicted (prelab) Range of I_D		Measured Range of I_D	
	Low I_D	High I_D	Low I_D	High I_D
Gate Bias				
Self Bias				
Voltage Divider Bias				
Current Source Bias				

2) Look at the measured range of I_D. and compare the results for each bias type. What can you conclude about each circuit's ability to control I_D

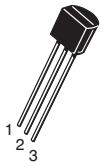
MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by MPF102/D

JFET VHF Amplifier
N- Channel – Depletion



MPF102



CASE 29-04, STYLE 5
TO-92 (TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	25	Vdc
Drain - Gate Voltage	V_{DG}	25	Vdc
Gate - Source Voltage	V_{GS}	-25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate - Source Breakdown Voltage (I_G = -10 mAdc, V_{DS} = 0)	$V_{(BR)GSS}$	-25	–	Vdc
Gate Reverse Current (V_{GS} = -15 Vdc, V_{DS} = 0) (V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)	I_{GSS}	– –	-2.0 -2.0	nAdc mAdc
Gate ±Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 2.0 nAdc)	$V_{GS(off)}$	–	-8.0	Vdc
Gate ±Source Voltage (V_{DS} = 15 Vdc, I_D = 0.2 mAdc)	V_{GS}	-0.5	-7.5	Vdc
ON CHARACTERISTICS				
Zero- Gate ±Voltage Drain Current(1) (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	2.0	20	mAdc
SMALL±SIGNAL CHARACTERISTICS				
Forward Transfer Admittance(1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$\|y_{fs}\|$	 2000 1600	 7500 –	µmhos
Input Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$Re(y_{is})$	–	800	µmhos
Output Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$Re(y_{os})$	–	200	µmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	–	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	–	3.0	pF

1. Pulse Test; Pulse Width ≤ 630 ms, Duty Cycle ≤ 10%.

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