Lab 1 Biasing methods to Achieve a Stable Q-Point

Name _____ **Section** _____

Purpose:

* To examine different types of bias used to set up a stable operating point.
* To sketch and label a DC load line for a transistor bias.

Equipment:

1- DMM
1- dc micro ammeter
1- dc voltmeter
1- dc Power Supply
Meter and Test Leads
3- Transistors - 2N3904 NPN (Q_1, Q_2, Q_3)
Resistors (330 Ω, 1 kΩ, 2 kΩ, 10 kΩ, 680 kΩ)

Pre-lab Preparation:

- Review sections 7.1, 7.2, & 7.3 of ***Introductory Electronic Devices and Circuits***

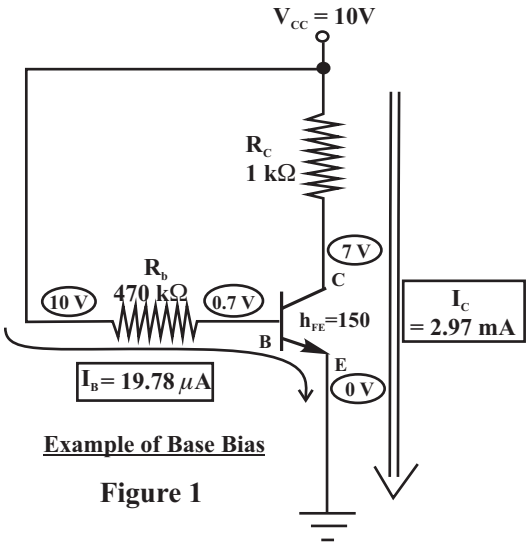
- Perform the dc analysis & complete the calculated portion of Tables 1 & 2.***Show all Calculations***
- Find $I_{C(sat)}$ & $V_{CE(off)}$ and plot the load line and plot the calculated Q point for both circuits.

Discussion: ***Base Bias***

The transistor has three regions of operation **;** ***saturation, active,*** and ***cutoff***.

The saturation region is when the transistor is in its totally "on" state. It is acting like a closed switch, and the collector current is at its maximum.

The cutoff region is when the transistor is in its totally "off" state. It is acting like an open switch and the collector current is at its minimum. (It should be very close to zero).



Example of Base Bias

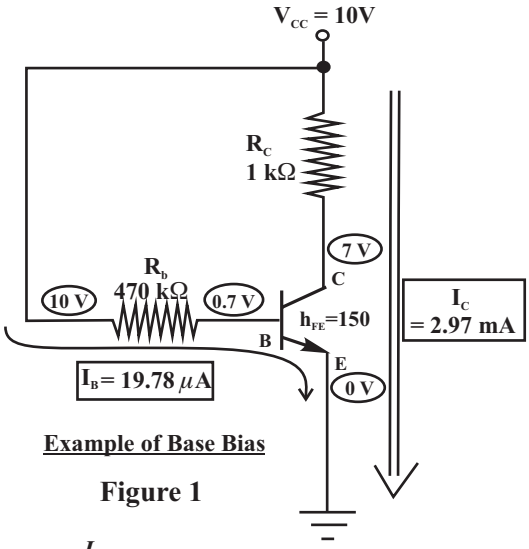
Figure 1

The active region is when the transistor is anywhere between saturation and cutoff. When it is in this region, the collector current is controlled by the base current. Remember that our transistor is basically a simple device. Look at Figure 1 to the right. It is an example of a ***Base Bias*** circuit. If we have a small amount of current flowing in the base circuit, we should have a larger current flowing in the collector circuit when the transistor is in the active region. The ratio between these two currents is called the dc current gain of the transistor (h_{FE}). In Fig. 1 the base current is 19.78 μA. This base current is determined by the value of R_B. The collector current is 2.97 mA. This is determined by the dc current gain of this transistor. Since this transistor has a current gain of 150, the collector current I_C, is 150 times larger than the base current. If this transistor had a gain of less than 150, then I_C would also be less. Conversely, if this transistor had a gain of more than 150, then I_C would be higher. As you can see, for a base bias circuit, I_C can be different for each transistor. The 2N3904 used here can have a current gain of anywhere from 100 to 300. This means that I_C can vary widely depending on the transistor we use. ***I_C is considered to be unstable*** because it can vary widely with different transistors of the same type.

Lab 1 Biasing methods

The Q Point and Midpoint Bias

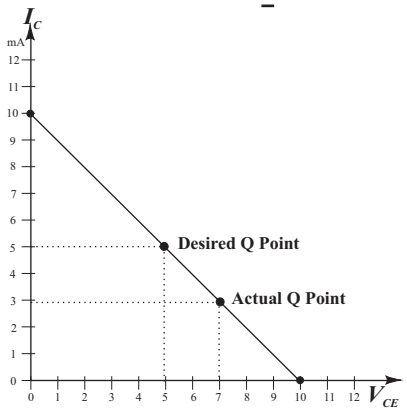
The Q point refers to the collector current. In the circuit shown in Fig. 1, the collector current is 2.97 mA. This is referred to as the Q point because the collector current will remain at 2.97 mA provided that no other voltages affect the circuit. In other words this means that a current of 2.97 mA will normally flow in the collector circuit with no signal applied. Our purpose here is to eventually use our transistor circuit as an amplifier. We need to have the Q point as close to the centre of the load line is possible. In the case in Fig. 1, the maximum collector current that can flow is 10 mA.($I_{C(sat)}$)This means the ideal Q point is at 5 mA. When the Q point is at 5 mA, the value of V_{CE} (the voltage from collector to emitter) will be ½ of V_{CC} or 5 V. Note that this is also at the midpoint.



Example of Base Bias

Figure 1

Look at Fig. 1. Is this particular circuit midpoint biased ? Your answer should be ***no***. We have already determined that midpoint bias for this circuit is when the collector current is 5 mA and V_{CE} is 5 V (½ V_{CC}). The Q point for this circuit is ***below the centre*** of the load line at I_C =2.97 mA and V_{CE} = 7 V. See the load line shown below.



DC Load Line for Figure 1

A Stable Q Point – Why do we need it?

It is important that our initial Q point be in the centre of the load line. If it is located higher up the load line, or lower down the load line, our signal output from the transistor will likely be distorted. The problem is that h_{FE} varies from transistor to transistor. Because of this, our ***Q point is unpredictable if we use the base bias circuit shown in Fig. 1.*** Remember that our purpose is to consistently produce a Q point that is near the centre of the load line. The base bias circuit just doesn't do it. The reason is that the Q point is dependent on the value of h_{FE}. We will attempt to prove this point with the circuit shown in Figure 2.

Base Bias

Dc analysis Worksheet (Pre Lab)

Using example 7.3 in the textbook as a guide , calculate I_B, I_{CQ}, and V_{CEQ} for the circuit shown in Figure 2. Insert your answers on the ***Calculated Values*** line in Table 1. ***Show all Calculations***

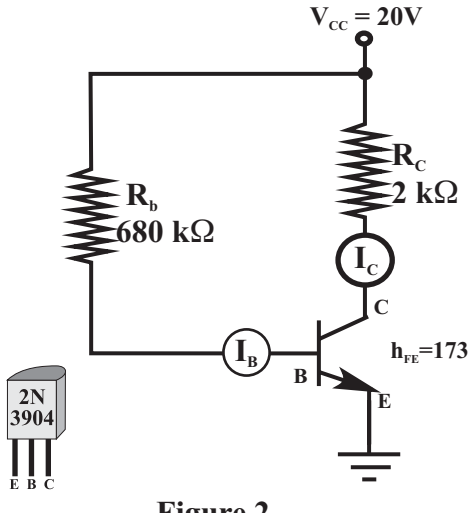


Figure 2

Lab 1 Biasing methods

Table 1 Base Bias	I_B	I_{CQ}	V_{CEQ}
Calculated Values			
Measured Values for Q_1			
Measured Values for Q_2			
Measured Values for Q_3			

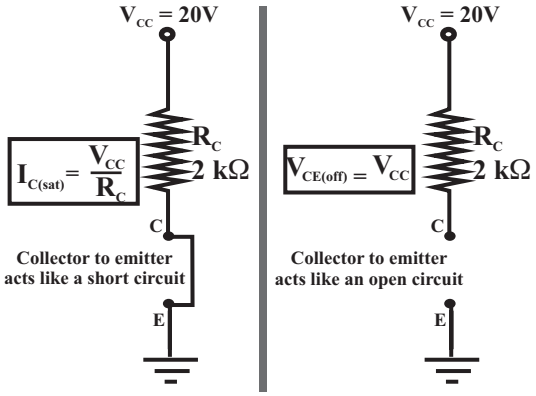
■***Plot the load line for the base biased circuit shown in Figure 2 (Pre-Lab)***

- Find both ends of the load line, plot these values, then draw a straight line to join the points.

Find $I_{C(sat)}$

$I_{C(sat)}$ is the maximum current that can flow when the transistor is saturated. This means that the transistor is acting like a closed switch as shown to the right. At this end of the load line, I_C is at its maximum and V_{CE} is near zero.

$I_{C(sat)}$ _____



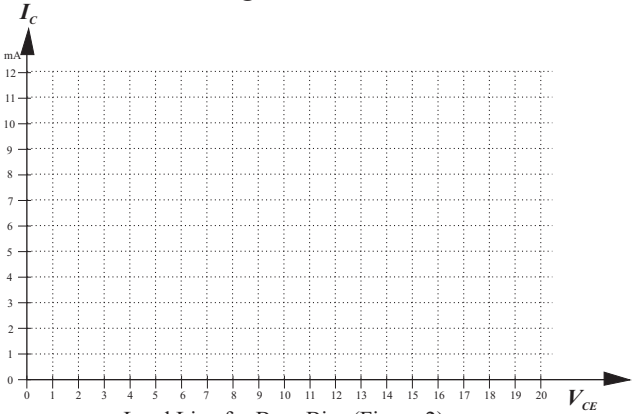
Finding the ends of the Load Line
Figure 3

Find $V_{CE(off)}$

$V_{CE(off)}$ is the voltage that appears across the transistor from collector to emitter when the transistor in acting like an open switch. $V_{CE(off)}$ is V_{CC} when the transistor is in this region. The collector current is nearly zero when the transistor is in cutoff.

$V_{CE(off)}$ _____

Plot the load line on graph to the right.
Plot your calculated Q point on the graph and label it.



Load Line for Base Bias (Figure 2)

Procedure: ***Do this part in the Lab***

1) Build the circuit shown in Figure 2 on your breadboard.

2) Measure the value of I_B, I_C, and V_{CE}. Record these values in Table 1 in the row for Q_1.

3) Repeat the above for Q_2 and Q_3.

4) Plot the measured Q points for all three transistors on the load line you created above. Label the Q points Q_1, Q_2, Q_3

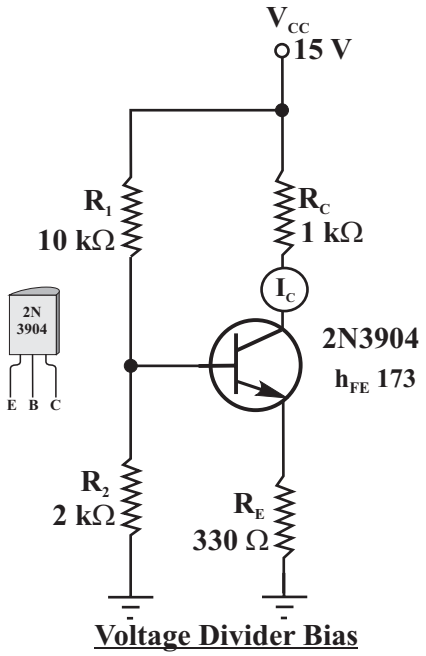
Lab 1 Biasing methods

Voltage Divider Bias

Discussion

Voltage divider biased provides us with a much more Stable Q- point. With this type of bias, the h_{FE} of the transistor plays no part in determining the Q point. In this circuit, it is the ***emitter resistor R_E that determines the collector current***.

This means that we can expect the Q-point to fall on the load line in the same place when we change the transistor to another of the same type. The following exercise will show this.



Voltage Divider Bias

Figure 4

Dc analysis worksheet (Pre-Lab)

Using example 7.11 in the textbook as a guide , calculate V_B, V_E, I_{CQ}, and V_{CEQ} for the circuit shown in Figure 4.

Insert your answers on the ***Calculated Values*** line in Table 2.

Show all Calculations

Table 2 VDB Bias	V_B	V_E	I_{CQ}	V_{CEQ}
Calculated Values				
Measured Values for Q_1				
Measured Values for Q_2				
Measured Values for Q_3				

Lab 1 Biasing methods

Dc analysis worksheet (Pre-Lab continued)

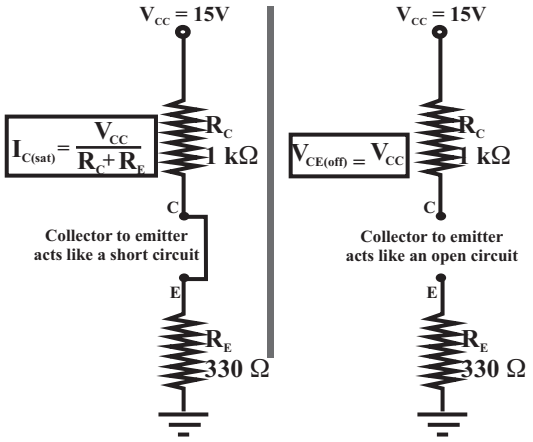
Plot the load line for the Voltage Divider Bias Circuit shown in Figure 4 (Pre-Lab)

1) Find both ends of the load line, plot these values, then draw a straight line to join the points.

Find $I_{C(sat)}$

$I_{C(sat)}$ is the maximum current that can flow when the transistor is saturated. This means that the transistor is acting like a closed switch as shown to the right. At this end of the load line, I_C is at its maximum and V_{CE} is at zero. The current flowing in the circuit is determined by the total resistance in the circuit. Notice that this time, there are two resistors in the circuit. The total resistance is the addition of these.

$I_{C(sat)}$ _____



Finding the ends of the Load Line for VDB
Figure 5

Find $V_{CE(off)}$

$V_{CE(off)}$ is the voltage that appears across the transistor from collector to emitter when the transistor in acting like an open switch. $V_{CE(off)}$ is V_{CC} when the transistor is in this region. The collector current is zero when the transistor is in cutoff.

$V_{CE(off)}$ _____

Plot the load line on graph below. Plot your calculated Q point on the graph and label it.

Procedure: Voltage Divider Bias
Do this part in the Lab

1) Build the circuit shown in Figure 4 on your breadboard.

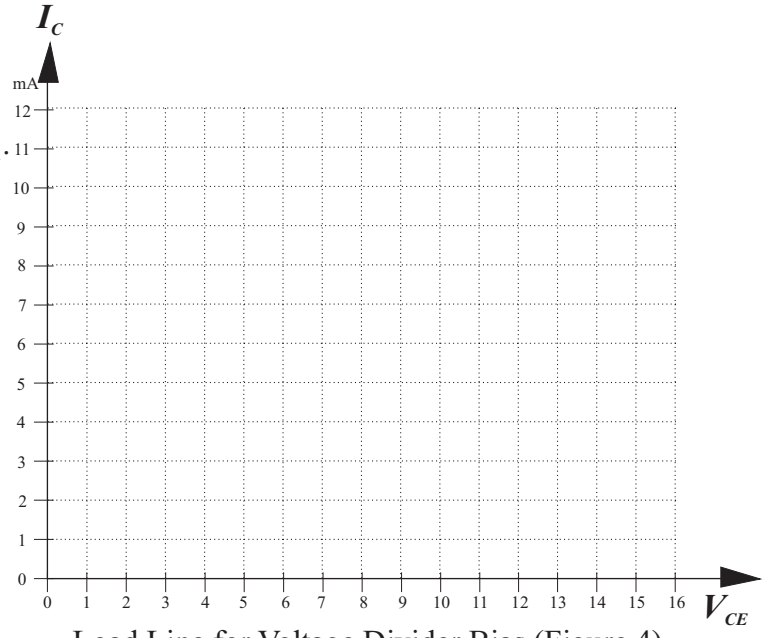
2) Measure the value of V_B, V_E, I_{CQ}, and V_{CEQ}. Record these values in Table 2 in the row for Q_1.

3) Repeat the above for Q_2 and Q_3.

4) Plot the measured Q points for all three transistors on the load line you created above.

5) Label the Q points Q_1, Q_2, Q_3.

(The Q points should plot almost on top of each other.)



Load Line for Voltage Divider Bias (Figure 4)