Technical Feature

Optimum Design for Linearity and Efficiency of a Microwave Doherty Amplifier Using a New Load Matching Technique

A Doherty amplifier with full load matching circuits of the carrier and peaking amplifiers at both low and high power levels is demonstrated for the first time. In the circuit design, sections of transmission lines are inserted in the load matching network for power-level-dependent load impedances. The circuit elements and bias points are designed and optimized using a large-signal harmonic balance simulation to offer simultaneous improvements in linearity and efficiency. Two 1.4 GHz Doherty amplifiers have been implemented using silicon LDMOS FETs. The RF performances of the Doherty amplifier-I (a combination of a class B carrier amplifier and a bias-tuned class C peaking amplifier) have been compared with those of a class B amplifier alone. The Doherty amplifier-II (a combination of a class AB carrier amplifier and a bias-tuned class C peaking amplifier) has been compared with a class AB amplifier alone. The new Doherty amplifiers show an improved linearity as well as higher efficiency.

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High efficiency and good linearity have become important figures of merit for power amplifiers used in CDMA basestations. Thermal problems arise as the operational power level of the amplifier is gradually increased and its size becomes more and more compact. The microwave Doherty amplifier is a good candidate for this use and much literature has been written about it. It was first proposed to improve efficiency by using an active load-pull technique on a carrier amplifier through a quarter-wave length line impedance transformer.[1-3] Because a quarter-wave length line is used for the load-pull and input splitter circuits for the parallel combination of the carrier and peaking amplifiers, MMIC implementations of the Doherty amplifier have been reported at very high frequencies (a few tens of gigahertz).[4-6] MIC implementation may be appropriate for the microwave Doherty amplifier at a few gigahertz for basestation application.

The advantages and disadvantages of the microwave Doherty amplifier have been addressed in previous reports.[3-8] Its well-known advantages are:

- Simplicity: The microwave Doherty amplifier can be realized using pure RF techniques to improve efficiency without using complex sub-paths and envelope control circuits used in envelope elimination and restoration (EER) and envelope tracking.
- High efficiency: The load-pull technique, using a quarter-wave transmission line, can deliver an efficiency comparable to other methods such as EER and envelope tracking.
- Ease of additional linearization using conventional methods: Conventional linearization, such as feedforward and envelope feedback, can still be used easily.

The well-known disadvantages are:

- Narrow bandwidth caused by the quarter-wave transformer. However, the bandwidth of modern wireless communication systems is sufficiently narrow and this is not a limiting factor.
- Poor output SWR: This is not a problem for most of the basestation power amplifiers because an isolator placed at the output guarantees good SWR.

- Resistive load matching: It was believed that only a resistive load-pull is possible in a microwave Doherty amplifier. However, a load matching technique is proposed, which includes reactive impedances by adding offset transmission lines in the load-pull circuit.
- Poor inter-modulation distortion (IMD) performance: The peaking amplifier may generate a large distortion due to a low biasing condition (class B or C). The distortion components of the peaking amplifier can be canceled by the distortion components generated by the carrier amplifier if the bias condition is properly adjusted. The cancellation mechanism will be explained later in this article using gain flattening.
- Gain degradation: This is due to the class B or C peaking amplifier. However, the gain degradation can be kept low (within 2 dB, as shown experimentally) because the gain of the carrier amplifier increases at low power levels due to the load-pull (higher gain resulting from the higher load impedance).

In this article, a new design technique is presented to fully match the resistive as well as reactive load impedance of the microwave Doherty amplifier for different power levels using offset transmission lines in the load-pull network. The linearity can be optimized by adjusting the length of the offset lines and the gate bias of the peaking amplifier, as demonstrated in the experiments. At the optimum linearity points, the efficiency is somewhat degraded in comparison to the ideal Doherty characteristics, but is still better than for the conventional classes. For the experiments, a 1.4 GHz microwave Doherty amplifier was designed and optimized using a large-signal model simulation. The efficiency and linearity of the Doherty amplifier was evaluated for the two modes of operation: Mode-I is a combination of a class B carrier amplifier and a bias-tuned, class C peaking amplifier, and Mode-II is a combination of a class AB carrier amplifier and a bias-tuned, class C peaking amplifier. They are compared with conventional class B and AB amplifiers for various signals (one-tone, two-tone and forward-link CDMA signals), respectively. The efficiency and linearity are simultaneously improved in the new Doherty amplifiers for the CDMA signal with high peak-to-average ratio (11 dB). The design technique and the measured performance of the microwave Doherty amplifiers are presented.

Design and Implementation

Basic Operation

The basic operation principle of a Doherty amplifier has been well described in the literature.[1-6] ***Figure 1*** shows the schematic diagram of a conventional Doherty amplifier. The Doherty amplifier has three operation modes: low, medium and high input power drive. In the low input power drive mode, when the same size devices for the carrier and peaking amplifiers are used, the load impedance of the carrier amplifier is doubled to $2R_0$ by the impedance transformer. The gain and efficiency are enhanced by the high load resistance. In the high input power drive mode, the load impedance of the carrier amplifier becomes R_0 because the peaking amplifier is turned on. At the medium input power drive, the load impedance of the carrier amplifier varies from $2R_0$ to R_0 according to the input drive level. By using a larger size device for the peaking amplifier than that for the carrier amplifier, a load variation factor greater than two can be achieved.

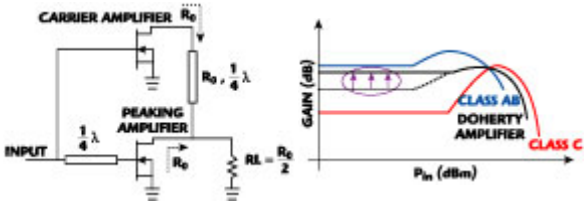

Fig. 1 Conventional Doherty amplifier

Fig. 2 Gain characteristics of a

circuit diagram. conventional Doherty amplifier.

Generally, the carrier amplifier and peaking amplifier have different operating classes. The gain characteristic of a Doherty amplifier using a parallel combination of class AB and C amplifiers is shown in ***Figure 2*** . The gain characteristics can be linearized by compensating the saturation response of the class AB carrier amplifier by turning on the class C peaking amplifier. The gain expansion caused by the high load impedance of the carrier amplifier in the low power drive mode can further flatten the gain characteristics of the amplifier. However, the signal clipping at the output of the peaking amplifier must not generate excessive higher order inter-modulation terms while improving linearity. Therefore, care should be made to optimize the linearity of the microwave Doherty amplifier by adjusting the bias level of the peaking amplifier.

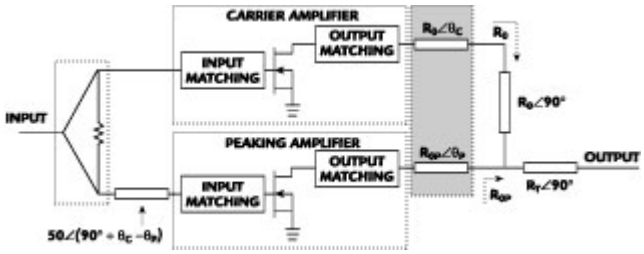

Fig. 3 Schematic diagram of the proposed Doherty amplifier.

Design

Figure 3 shows the schematic diagram of the proposed fully matched microwave Doherty amplifier with offset transmission lines in the input and output circuits. The carrier and peaking amplifiers have input and output power matching circuits, which transform the input impedance to 50 W and the output impedance to R_0 for the carrier amplifier, and R_{0P} for the peaking amplifier at a high power operation. The additional offset transmission lines, having characteristic impedances of R_0 and R_{0P} at the output and 50 W at the input, do not affect the overall matching conditions for high power operation because they are matched to the characteristic impedances and are designed to have equal phase delays. However, the offset components at the output, with a proper delay, deliver the higher output impedance matching at the low power level. The quarter-wave impedance transformer with a characteristic impedance of R_T is inserted to transform the combined load impedance to 50 W. The device size ratio between the carrier and peaking amplifier determines the characteristic impedance ratio between them. The relation can be given by

$$R_{0P} = \frac{R_0}{\alpha} \qquad (1)$$

where
a = size ratio of the peaking amplifier to the carrier amplifier

For the same size of carrier and peaking amplifiers, R_{0P} becomes R_0 . The characteristic impedance R_T is calculated as

$$R_T = \sqrt{\frac{50R_0R_{0P}}{R_0 + R_{0P}}} = \sqrt{\frac{50R_0}{1+\alpha}} \qquad (2)$$

In this experiment, the same size for the peaking and carrier amplifiers was used for easy validation of the proposed technique. F. H. Raab previously reported the formula for the ideal efficiency characteristics of the amplifier with a peaking amplifier of a larger size.[2]

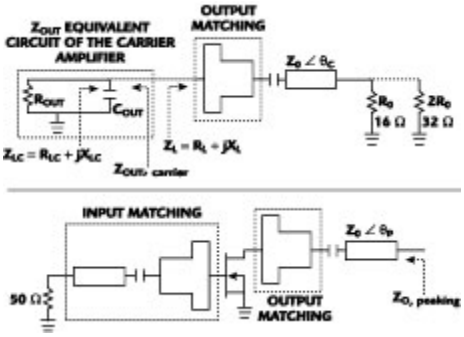

Fig. 4 Load matching techniques to determine the angle of the offset transmission line for the (a) carrier and amplifier and (b) peaking amplifier.

Figure 4 shows the circuit diagrams to determine the lengths of the offset lines for the carrier and peaking amplifiers. The load impedance matched to have the highest output power has both a resistive and reactive value, which is plotted as $Z_{L,\,R0}$ in ***Figure 5*** . For the Doherty operation at very low power level, the load impedance $Z_{L,2R0}$ form a circle around the center point $Z_{L,R0}$, according to the various angles of the offset line, resulting in complex values. It is impossible to find out the optimum point of load impedance at low power levels just by observing these complex values. To obtain the optimum phase offset of the carrier amplifier, the output equivalent circuit of the carrier amplifier with a shunt resistor R_{out} and a capacitor C_{out} is used. C_{out} and R_{out} at the high power mode are determined by the condition that the compensated load impedance $Z_{LC,R0}$ is moved from $Z_{L,R0}$ to a pure real value for the R_0 load termination. In the present case, the optimum C_{out} is 8.2 pF and R_{out} is 23.5 W. At the low power level, $Z_{LC,2R0}$ with the $2R_0$ load termination forms a circle around $Z_{LC,R0}$. Then, the optimum offset angle can be chosen for the $Z_{LC,2R0}$ to have a high resistive value of 43.8 W at 50°. The matching for the peaking amplifier can be designed in a similar way. The small-signal output impedance $Z_{o,peaking}$ of the peaking amplifier including input and output matching circuits and an offset transmission line component shows a circle according to the varying phase angle of the offset line, as shown in ***Figure 6*** . The optimum offset angle can be determined for the output impedance $Z_{o,peaking}$ to have a high resistive value of 114.4 W at 50°.

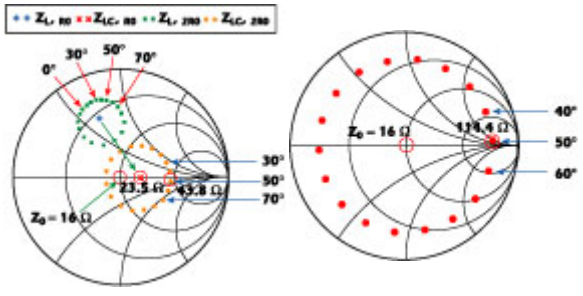

Fig. 5 Simulated results for the load and compensated load impedances for the carrier amplifier.

Fig. 6 Simulated output impedance of the peaking amplifier.

A large-signal harmonic balance simulation has been conducted to further optimize the linearity by tuning the initial offset values obtained by the previously described method and the gate bias level of the peaking amplifier. An LDMOS FET large-signal model[9] of Ericsson's PTF10107 was used in the simulation and implementation. The optimized values are 40.68° for both carrier and peaking amplifiers and are very similar to the initial values. The design procedure can be summarized as follows: carrier and peaking amplifiers design for power operation - determination of C_{out} and R_{out} for the load-pull - determination of phase offsets - final optimization for efficiency and linearity by tuning the gate bias conditions and the length of the offset lines. The bias optimization is very important for proper cancellation of inter-modulation terms generated by the carrier and peaking amplifiers; however, it can degrade the efficiency improvement.

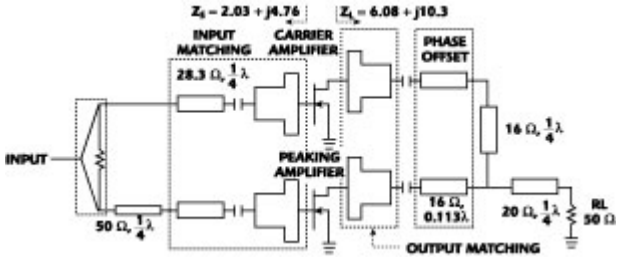

Fig. 7 Implemented circuit diagram for a 1.4 GHz Doherty amplifier using Si LDMOS FET.

Implementation

Figure 7 shows the circuit diagram of the implemented Doherty amplifier. Identical devices (5 W peak-envelope-power silicon LDMOS FETs) are used for both carrier and peaking amplifiers. The input and output of the amplifier are matched to 16 W using micro-strip open stubs to have source impedance (Z_s) of 2.03 + j4.76 W and load impedance (Z_L) of 6.08 + j10.03 W. The 16 W quarter-wave length line is used for the load-pull operation and the 20 W quarter-wave transformer is used for matching the combined two 16 W lines to 50 W. The input signal is split with a Wilkinson divider and a 50 W quarter-wave line is inserted in the input stage of the peaking amplifier to match the delay between the two paths. Additional 16 W lines (0.113l, 40.68°) are inserted at the output stages of both amplifiers as offset components to achieve the optimized performance. Because of the identical delays of load offset lines for the two amplifiers, an additional delay line at the input is not employed.

Experimental Results

Performance comparisons between the Doherty-I and class B amplifier, and between the Doherty-II and class AB amplifiers are performed. ***Figure 8*** shows the PAE of the Doherty-I, Doherty-II, class B and class AB amplifiers versus output power for a 1.4 GHz one-tone signal. The Doherty amplifiers have higher PAE throughout the wide output power range compared with the class B and AB amplifiers, respectively. This efficiency is a little lower than the expected efficiency of the ideal Doherty amplifier, which is caused mainly by a linearity optimization using bias adjustment of the peaking amplifier. The bias conditions of the amplifiers used in this experiment are summarized in ***Table 1*** .

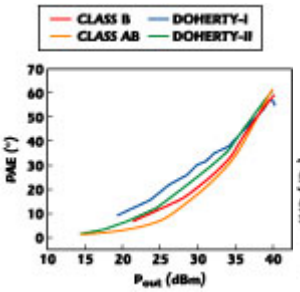

Fig. 8 Power-added efficiency for the Doherty-I, Doherty-II, class B and class AB amplifiers vs. output power for a single-tone, 1.4 GHz signal.

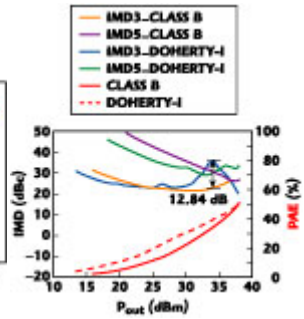

Fig. 9 IMD3, IMD5 and PAE vs. power output of the Doherty-I and class B amplifiers for a two-tone signal.

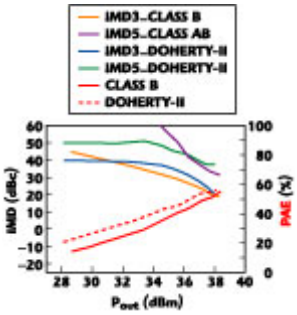

Fig. 10 IMD3, IMD5 and PAE vs. power output of the Doherty-II and class AB amplifiers for a two-tone signal.

The two-tone (1.400 GHz and 1.401 GHz, 1 MHz spacing) characteristics are also compared. Third-order inter-modulation distortion (IMD3), fifth-order inter-modulation distortion (IMD5) and PAE for the Doherty-I and class B amplifiers, and for the Doherty-II and class AB amplifiers versus average output power are compared in ***Figures 9*** and ***10*** , respectively. The Doherty amplifier-I clearly has better efficiency and an improved IMD3, with as much as a 12.84 dB improvement at an output power of 33 dBm. IMD5 is worse at a low power level but it becomes better at a high power level (above 33 dBm), in comparison with the class B amplifier. The Doherty amplifier-II also shows a better efficiency but has worse IMD3 and IMD5 at a low power level and is improved at a high power level in comparison with the class AB amplifier.

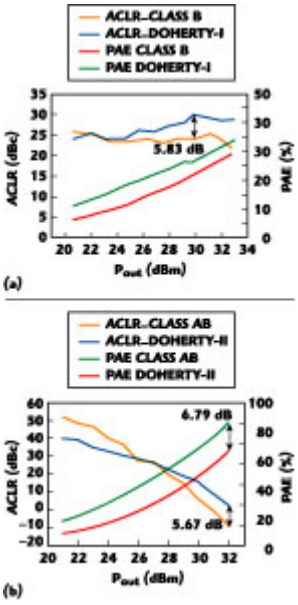

Fig. 11 ACLR at 885 KHz offset and the PAE vs. output power for a CDMA signal for the (a) Doherty-I and class B amplifiers and (b) Doherty-II and class AB amplifiers.

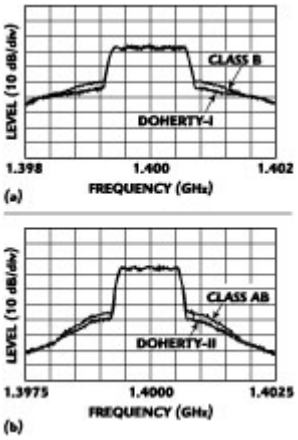

Fig. 12 Output CDMA spectra comparison for the (a) Doherty-I and class B amplifiers and (b) Doherty-II and class AB amplifiers.

CDMA test results are shown in ***Figure 11*** . The adjacent channel leakage ratio's (ACLR) at 885 kHz offset and PAEs versus average output power for the Doherty-I and class B amplifiers, and

of the Doherty-II and class AB amplifiers, are compared using a CDMA signal (forward-link, chip rate of 1.2288 Mcps and peak-to-average ratio of 11 dB). The Doherty amplifier-I shows a significantly improved efficiency and ACLR is improved by 5.83 dB at an output power of 30 dBm. The Doherty amplifier-II also has an efficiency improved by 6.79 percent with an ACLR reduced by 5.67 dB at an output power of 32 dBm. The Doherty amplifiers also clearly show improved linearity. This improved linearity and efficiency at a high power level can be expected since the gain change has been compensated for at high power levels by the peaking amplifier. The output spectra of the Doherty-I and class B amplifier at a 30 dBm output power, and Doherty-II and class AB amplifier at an output power of 32 dBm are shown in ***Figure 12*** .

Table 1
Experimental conditions including optimized biases and classes of operation of the amplifiers

Comparison I	
Doherty Amplifier I	Class B Amplifier
Carrier amplifier - class B (V_{gs} =3.6 V) Peaking amplifier - class C (V_{gs} =1.5 V)	V_{gs} =3.6 V
Comparison II	
Doherty Amplifier II	Class AB Amplifier
Carrier amplifier - class AB (V_{gs} =4.17 V) Peaking amplifier - class C (V_{gs} =2.8 V)	V_{gs} =4.17 V, I_{dsQ} =70 mA

Conclusion

A new simple load matching technique has been presented for the power-level-dependent varying load impedance of the microwave Doherty amplifier using offset transmission lines. This is the first demonstration of the Doherty amplifier with full load matching circuits, including resistive and reactive values of the carrier and peaking amplifiers, at both low and high power levels. Based on this concept, a 1.4 GHz microwave Doherty amplifier, using high power silicon LDMOS FETs, has been designed using a large-signal model. The model simulation provides the proper offset line values. The bias voltage is also adjusted during simulation for better cancellation of harmonics generated by the carrier and peaking amplifiers.

It is shown that there is a trade-off between linearity and efficiency in a microwave Doherty amplifier. The method to optimize the linearity by adjusting circuit components and gate bias of peaking amplifier with minimally sacrificing the improved efficiency using a load-pull technique has been demonstrated. The RF performances of the microwave Doherty amplifier for various input signals have been presented. The new Doherty amplifiers have delivered a simultaneously improved efficiency and linearity over the conventional class B or AB amplifiers for single-tone, two-tone and CDMA signals.

Acknowledgment

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